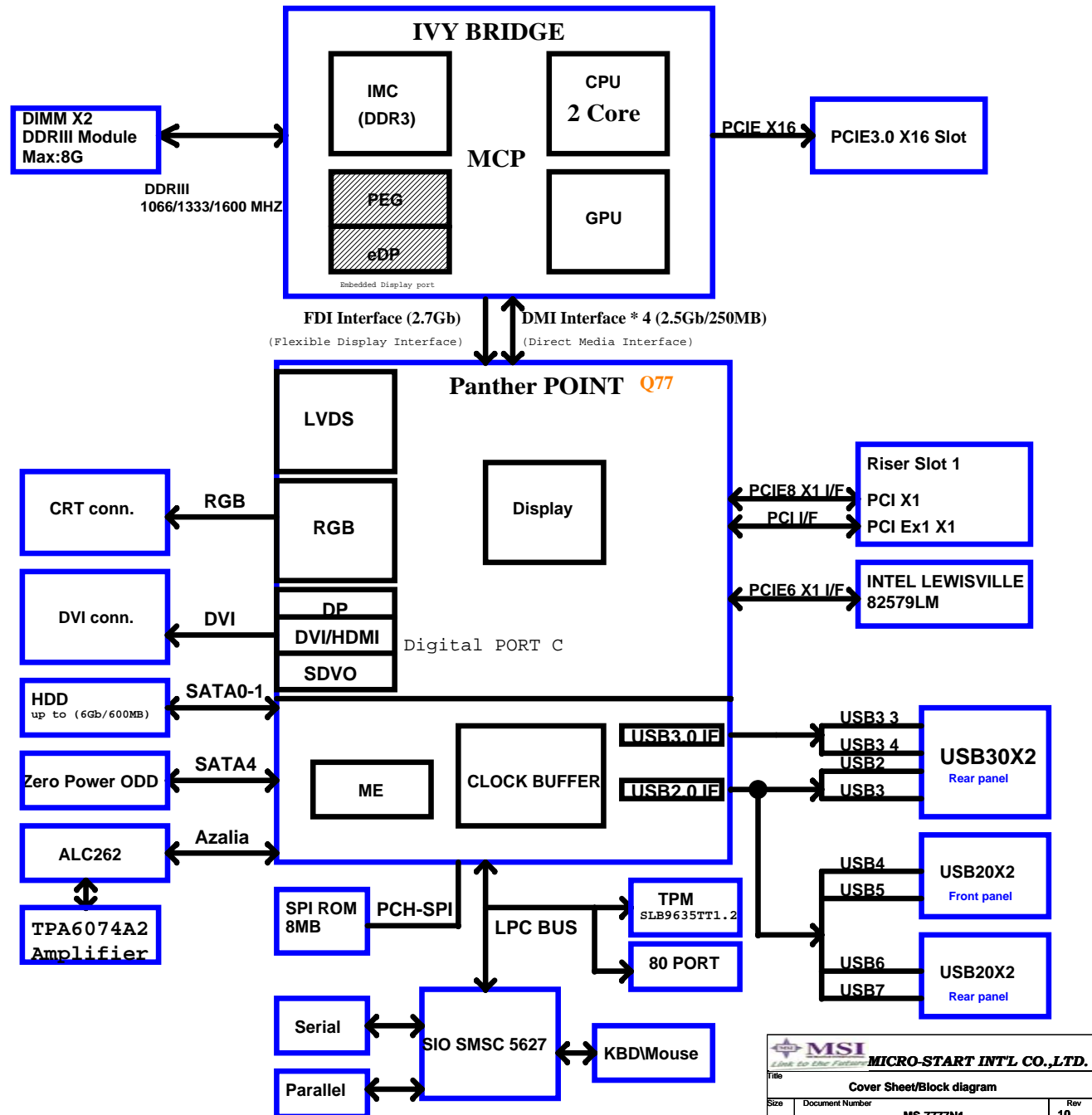
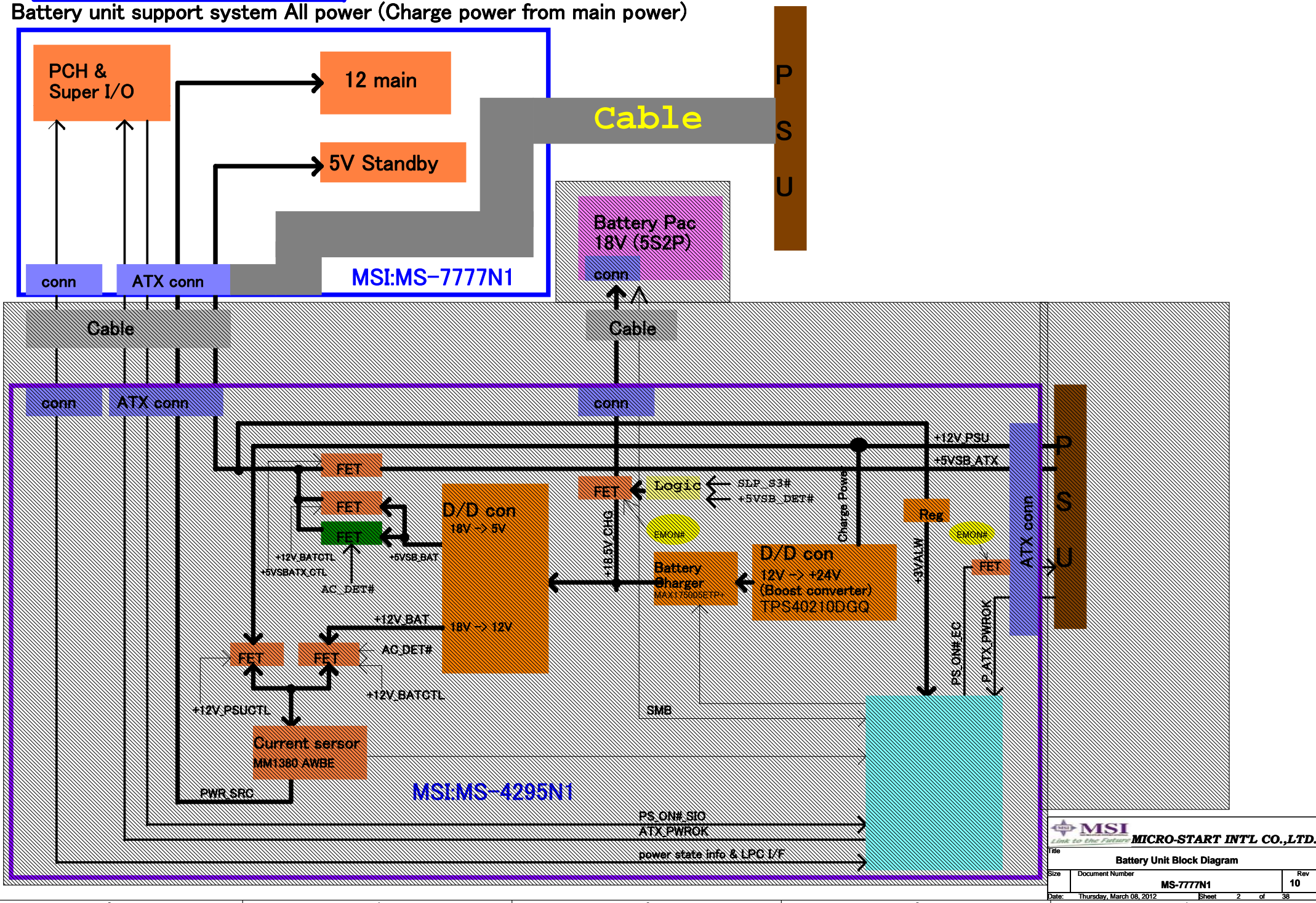


MSI:MS-7777N1 Ver : 10

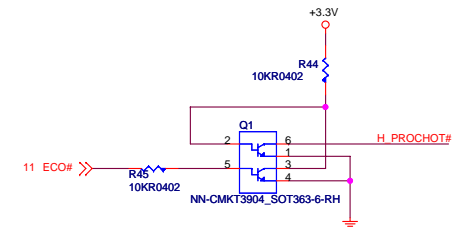


Battery Unit Diagram(Normal Sku)

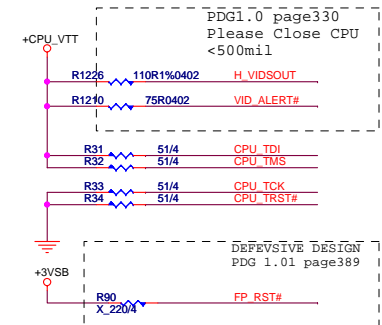
Battery unit support system All power (Charge power from main power)



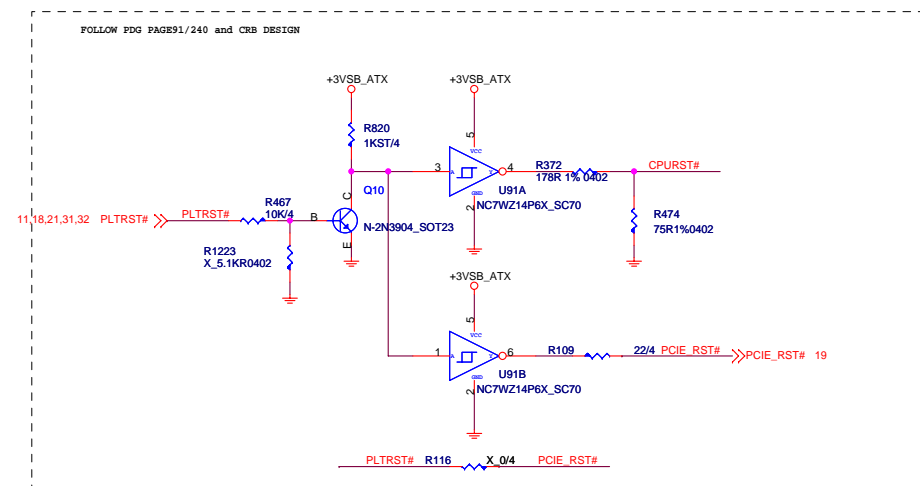
NEC ECO MODE



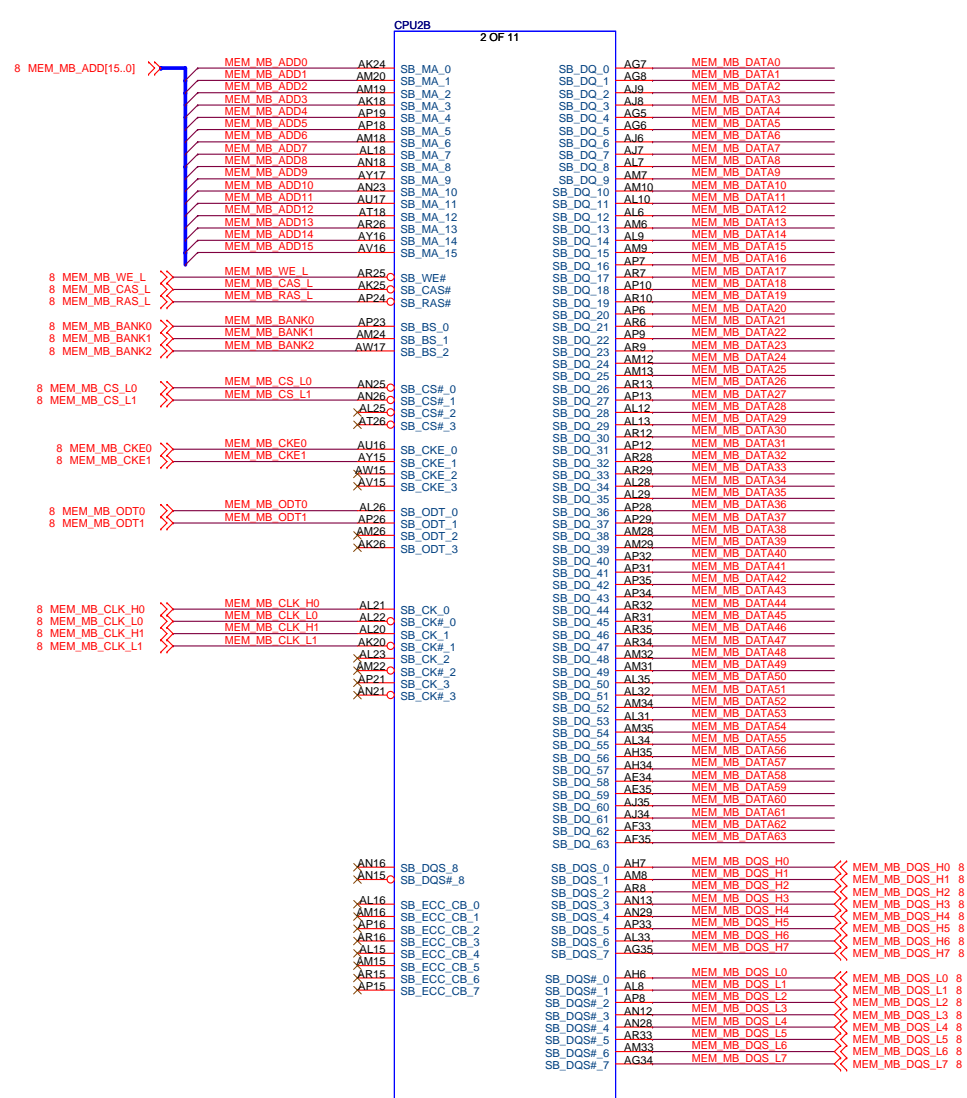
The diagram illustrates the CPU VTT circuit for the 10MW05. It shows a +CPU_VTT supply connected to a network of resistors (R21, R22, R23, R25, R26, R845) and capacitors (X 51/4, 1K51/4). The network is connected to various pins: CPURST#, H_PROCHOT#, H_CATERR#, H_THERMTRIP#, and CPU_PWRRD. A ground symbol is also shown connected to the network.



CPU RESET#

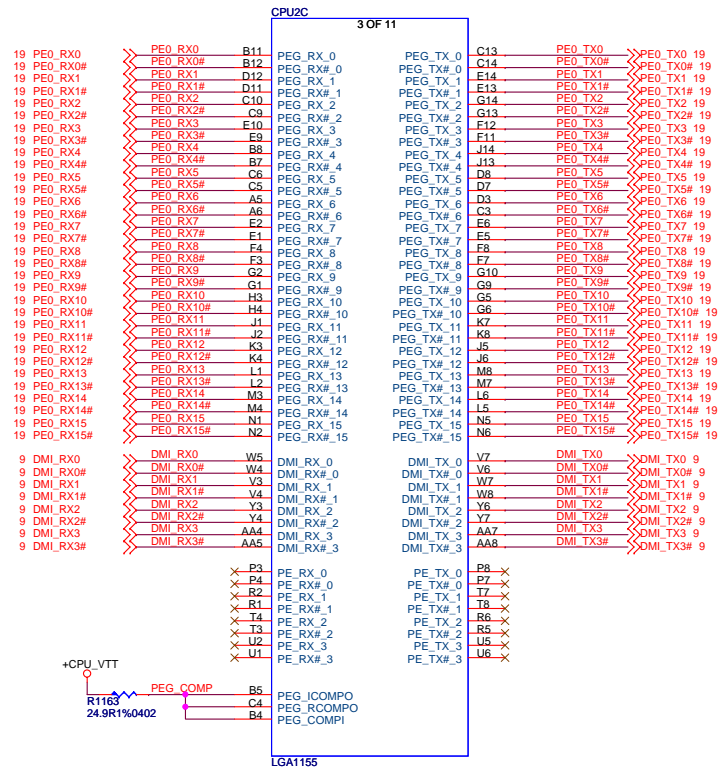


CPU Memory CH-B

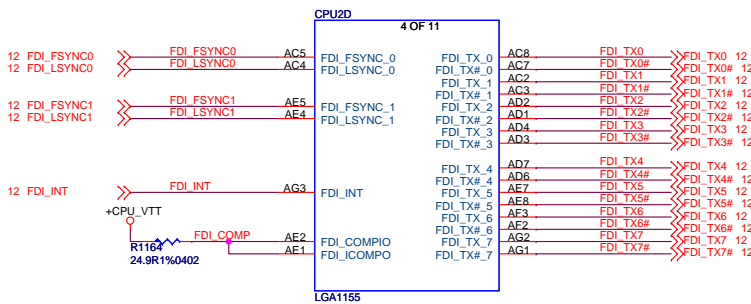


MEM_MB_DATA[63..0] << MEM_MB_DATA[63..0] 8

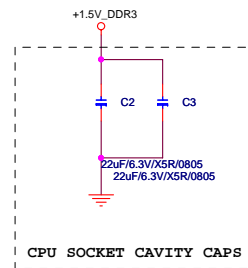
CPU-PCIE / DMI



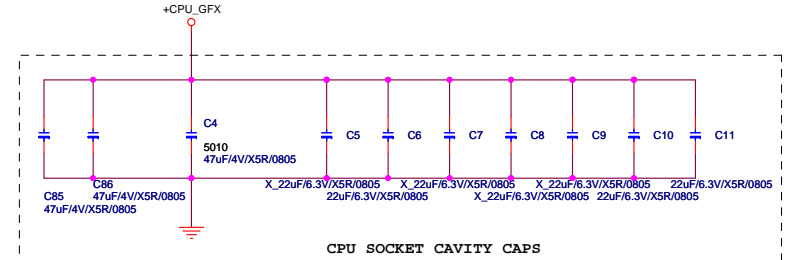
CPU-FDI



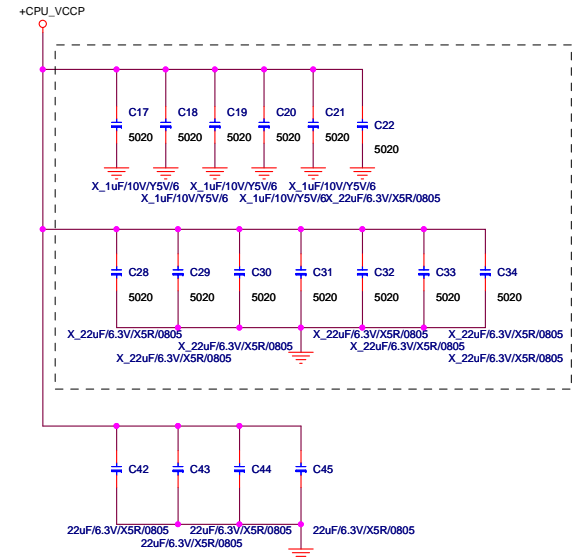
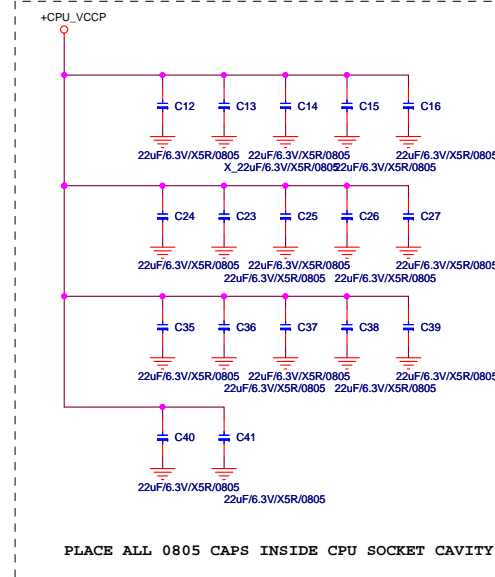
+1.5V_DDR3-Decoupling



+CPU GFX Decoupling

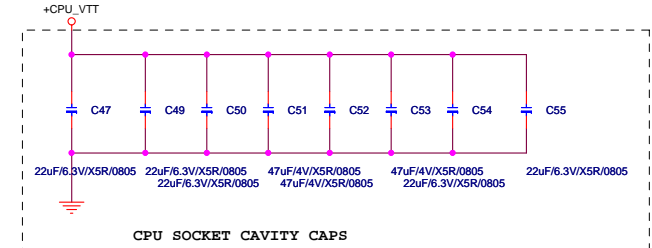


+CPU VCCP-Decoupling

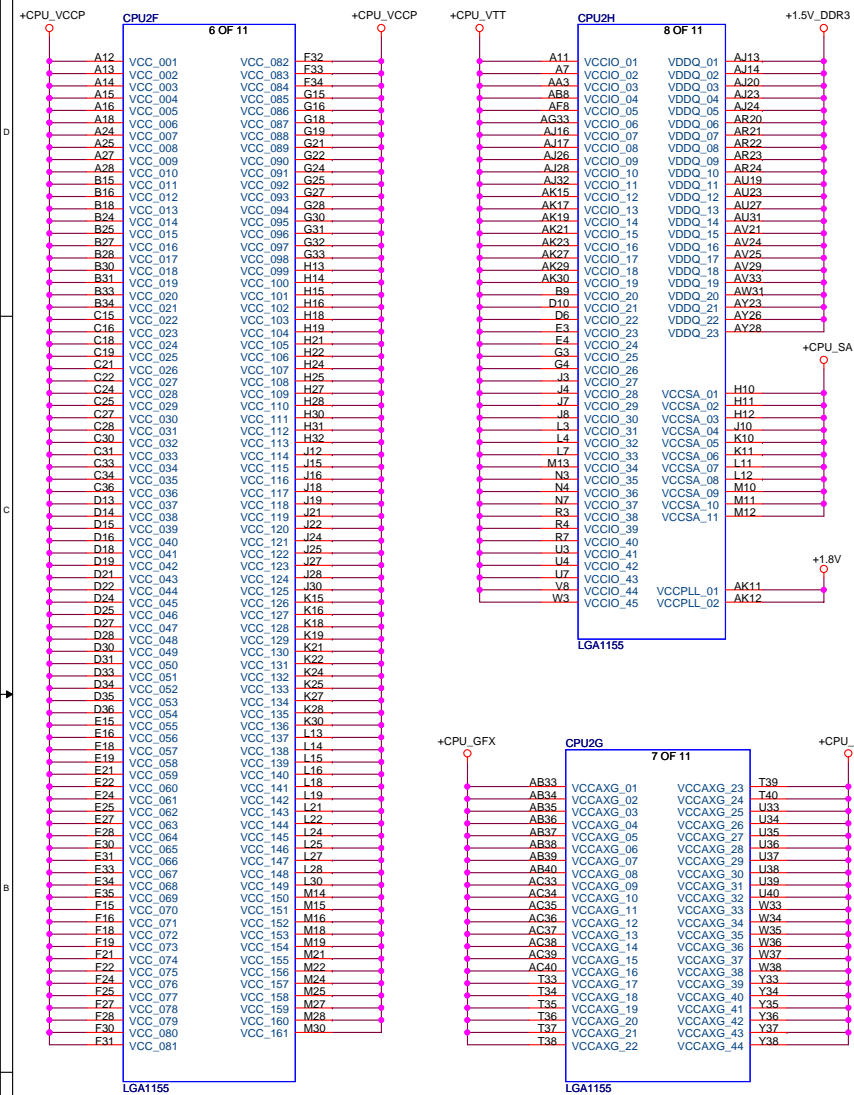


TOP SIDE ,CLOSE TO CHOKE

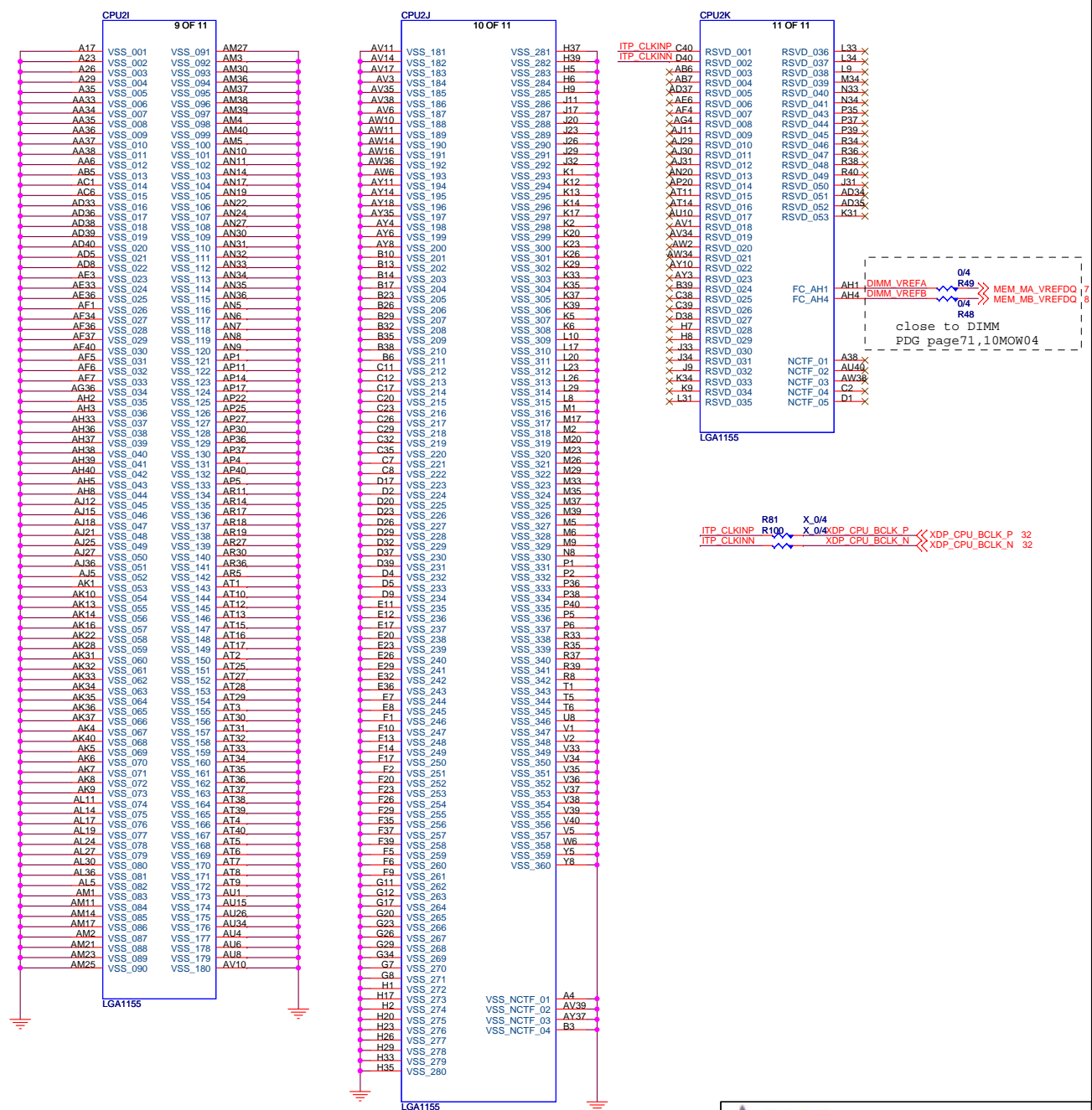
+CPU VTT Decoupling



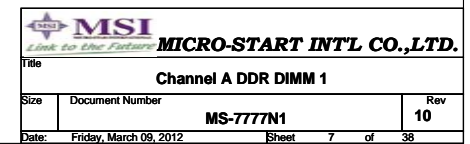
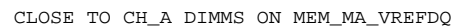
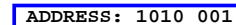
CPU-POWER



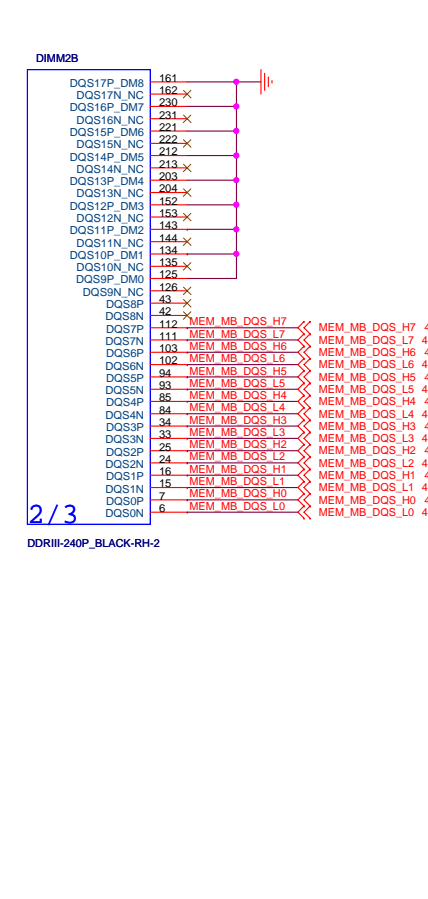
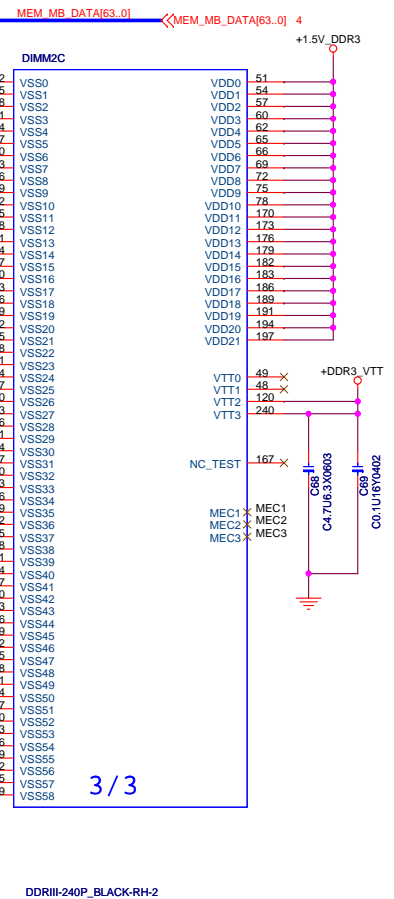
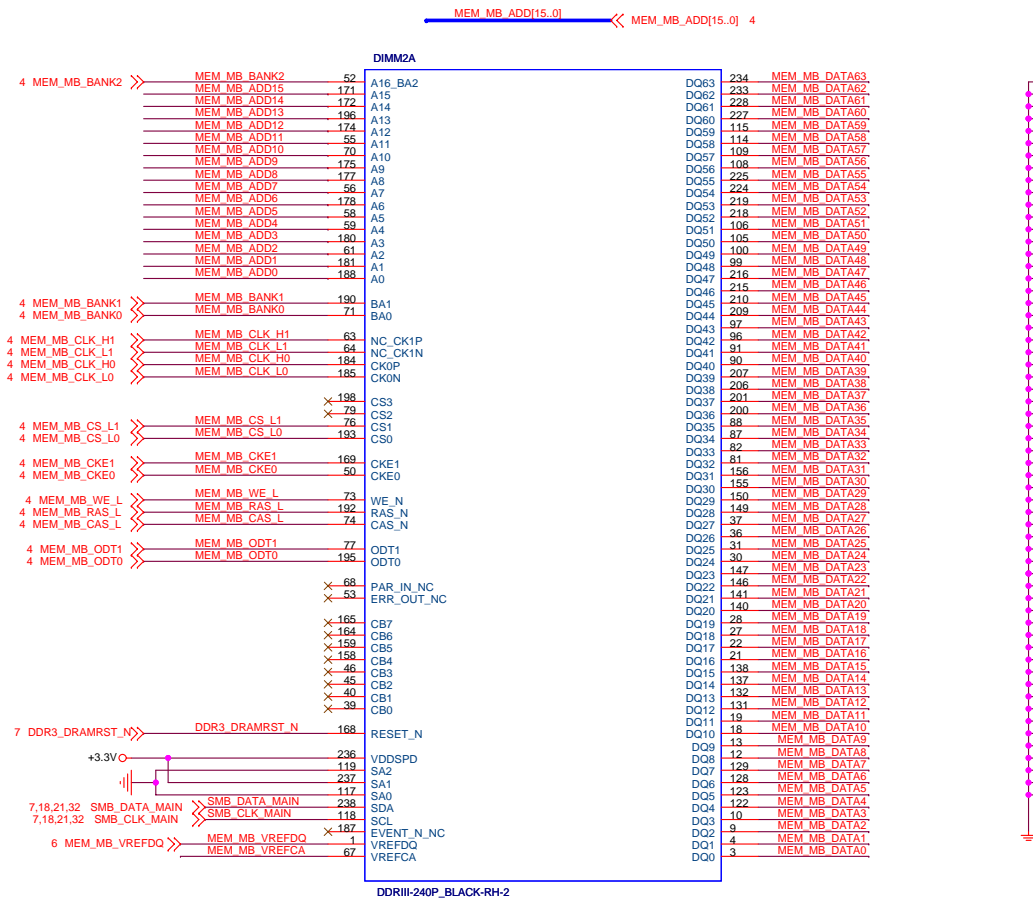
CPU-GND



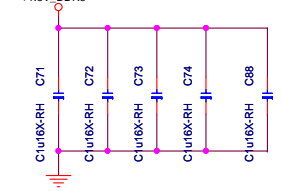
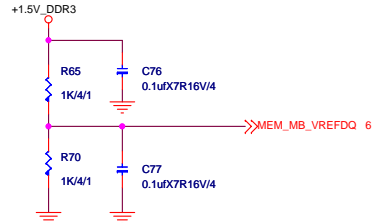
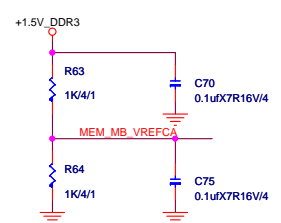
DDRIII CH-A DIMM1



DDRIII CH-B DIMM2

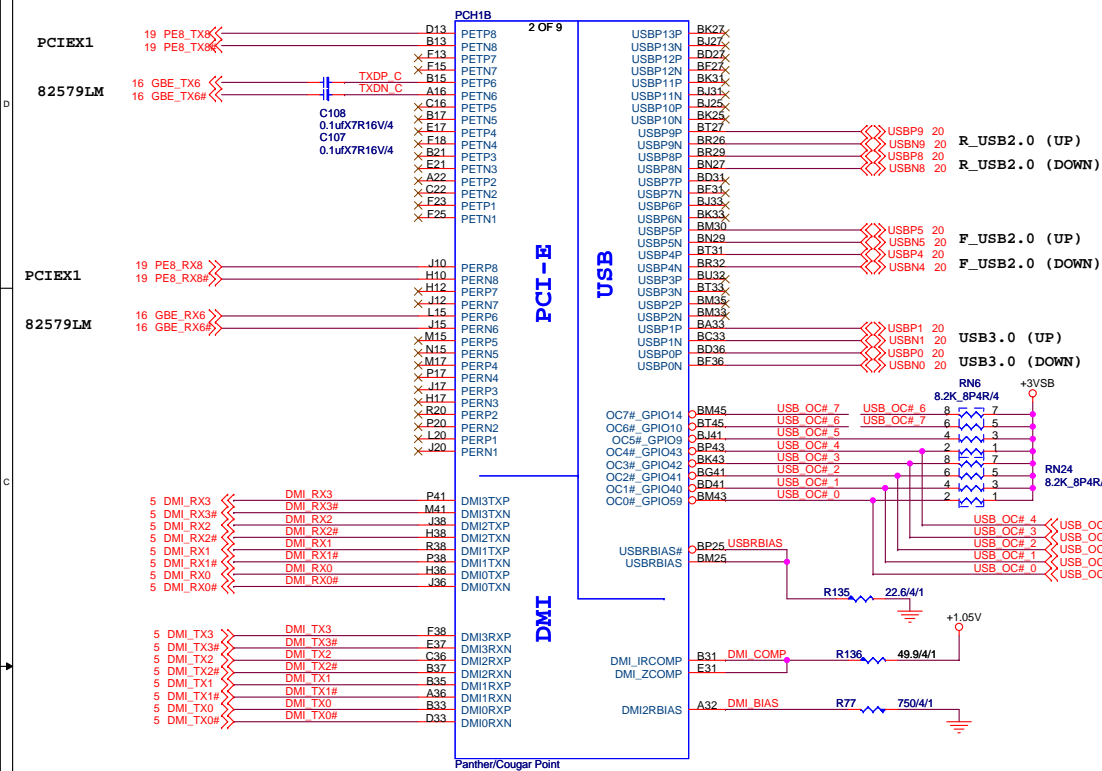


ADDRESS: 1010 010

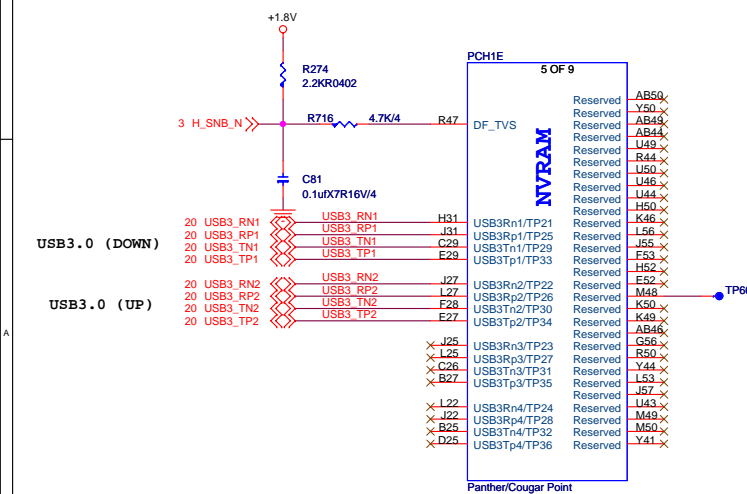


CLOSE TO CH_AB DIMMS ON MEM_MA_VREFDQ

PCH_PCIE/DMI/USB



USB3.0/NVRAM



DF TVS STRAP

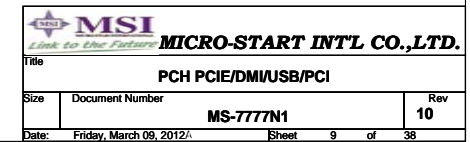
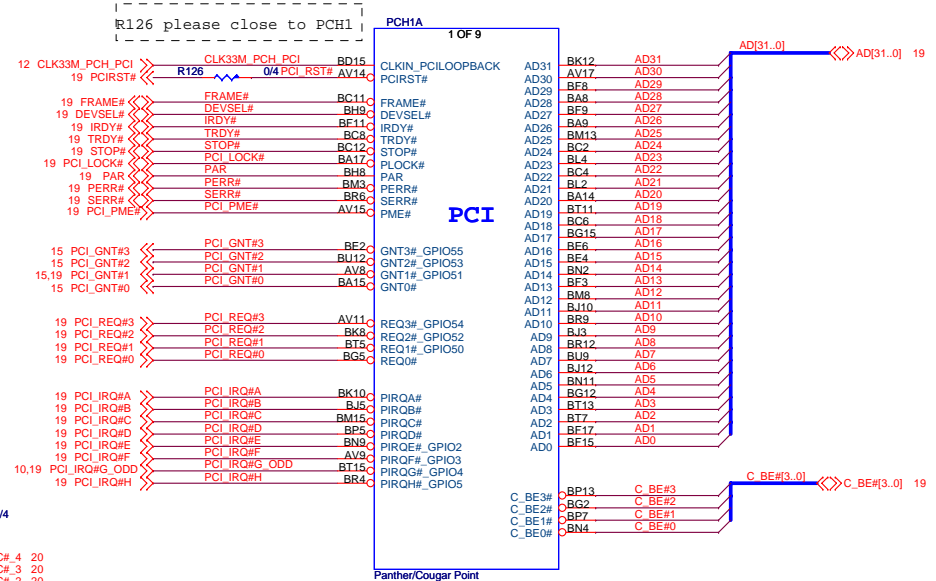
DF_TV5	DMI and FDI Tx/ Rx Termination Voltage
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This signal has a weak internal pull-down.
NOTE: The internal pull-down is disabled at deasserts.

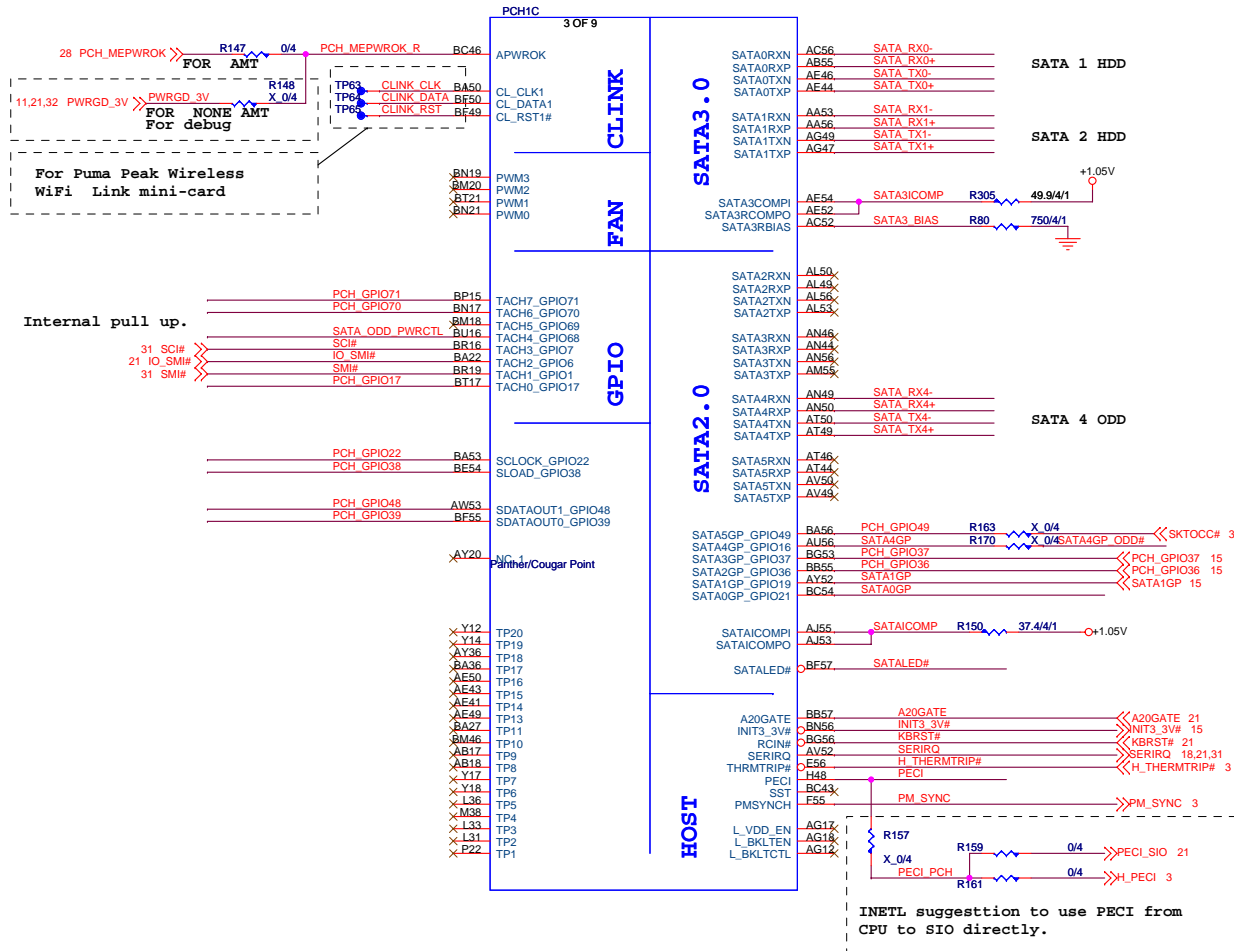
DMI & FDI Termination Voltage

NV_CLE	Set to Vss when LOW
	Set to Vcc when HIGH

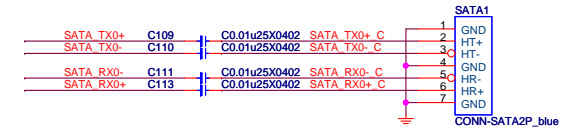
PCH PCI



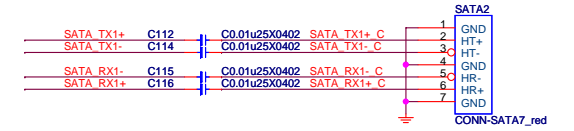
PCH SATAII/HOST/FAN/GPIO



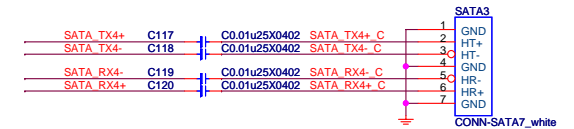
SATAIII CONN FOR HDD



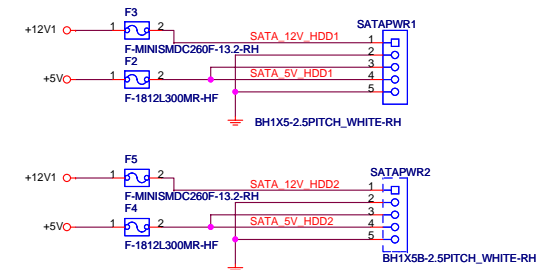
SATAIII CONN FOR HDD



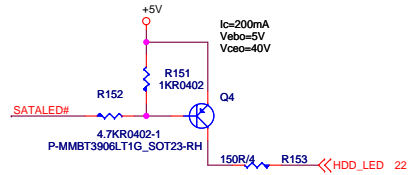
SATAII CONN FOR ODD



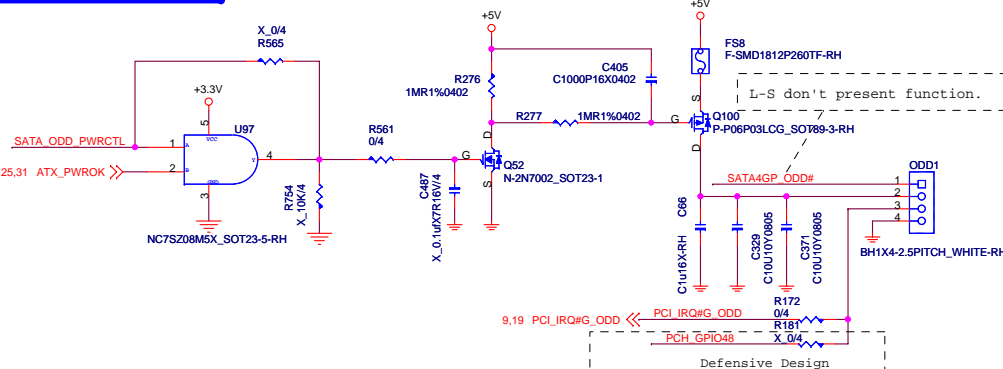
SATAII CONN POWER FOR HDD



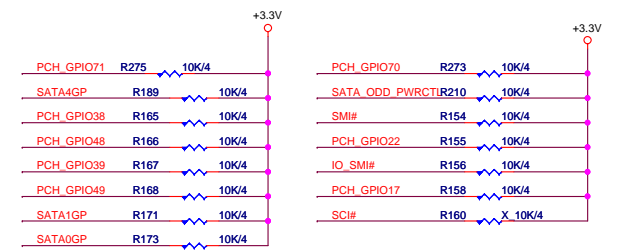
HDD_LED



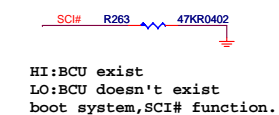
Zero Power ODD



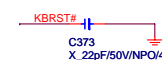
PULL UP RESISTOR



SCI#/Detect BCU exist



EMI



MSI

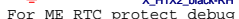
MICRO-START INT'L CO.,LTD.

File: **PCH SATA/HOST/GPIO/CLINK/ZERO ODD**

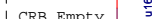
Size: Document Number **MS-7777N1** Rev **10**

Date: Friday, March 09, 2012/ Sheet 10 of 38

PCH1D

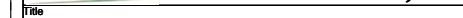


(1-2)	(2-3)
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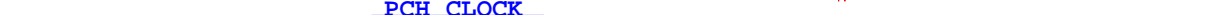
BCU_EXIST R408 47KR0402

HI:BCU exist
LO:BCU doesn't exist
boot system,SCI# function.



Size	Document Number	Rev
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PCW1E

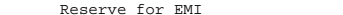


.....

PCH1G

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disabled after airplane accident



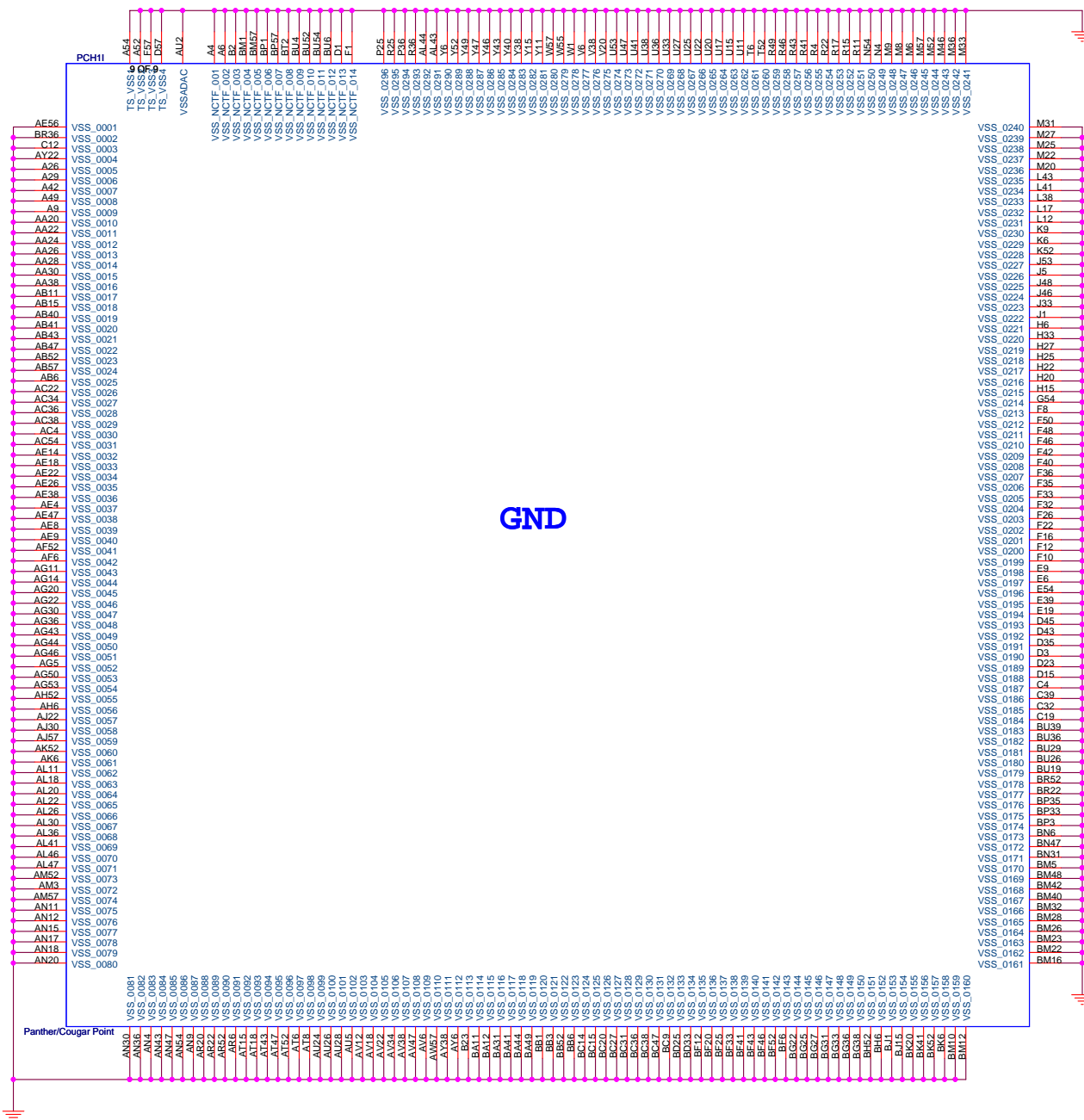
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PCH CLK/FDI/VA/HDMI/DP/SDVO

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	MS-000014	10

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PCH GND

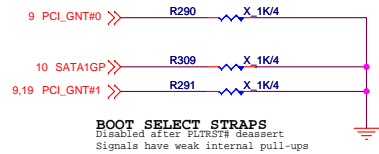


REQUIRED STRAPS

4/4146 EDS 1.0 page 94~97

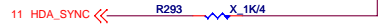
BOOT SELECT STRAPS

BOOT DEVICE	GNT1	GNT0/SATA1GP
LPC	0	0
NAND	0	1
SPI	1	1
PCI	1	0



HDA_SYNC STRAP

This signal has a weak internal pull-down.
On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.



GNT2#/GPIO53 STRAP

This Signal has a weak internal pull-up.
Tying this strap low configures DMI for ESI compatible operation.
NOTES:
1. The internal pull-up is disabled after PLTRST# deasserts.
2. ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.



GNT#3 STRAP

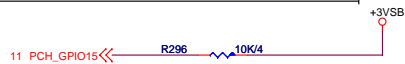
The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode (PCH inverts A16 for all cycles targeting BIOS space).
The status of this strap is readable using the Top Swap bit (Chipset Config Registers: Offset 3414h:Bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.



GPIO15-ME TLS STRAP

10MOW14

Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
High = Intel ME Crypto TLS cipher suite with confidentiality
This signal has a weak internal pull-down.
NOTE: The weak internal pull-down is disabled after RSMRST# deasserts.
NOTE: A strong pull-up may be needed for GPIO functionality



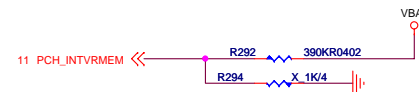
GPIO28 STRAP

This signal has a weak internal pull-up.
NOTE: The internal pull-up is disabled after RSMRST# deasserts.
The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.



INTVRMEN STRAP

Integrated 1.05 V VRMs is enabled when high
External VR power source is used for DcpSus when sampled low.
NOTE: External VR powering option is for Mobile Only. Other systems should not pull the strap low.



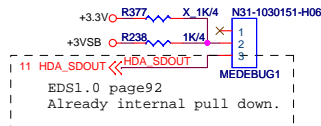
SPKR STRAP

The signal has a weak internal pull-down.
Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:Bit 5).



HDA_SDO ME STRAP

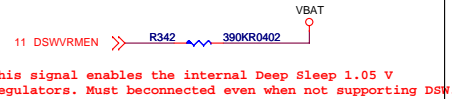
1-2: Default.
2-3: ME disable for FPRG.



NOTE: The weak internal pull-down is disabled after PLTRST# deasserts.
NOTE: Asserting the HDA_SDO high on the rising edge of RSMRST# will also halt Intel® Management Engine after chipset bringup and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.

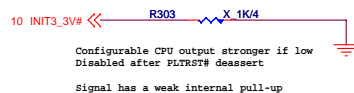
DSWVRMEN STRAP

If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.



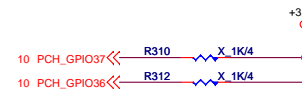
INIT3_3# STRAP

This signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled low



GPIO36/37 STRAP

This signal has a weak internal pull-down.
NOTES:
1. The internal pull-down is disabled after PLTRST# deasserts.
2. This signal should not be pulled high when strap is sampled.



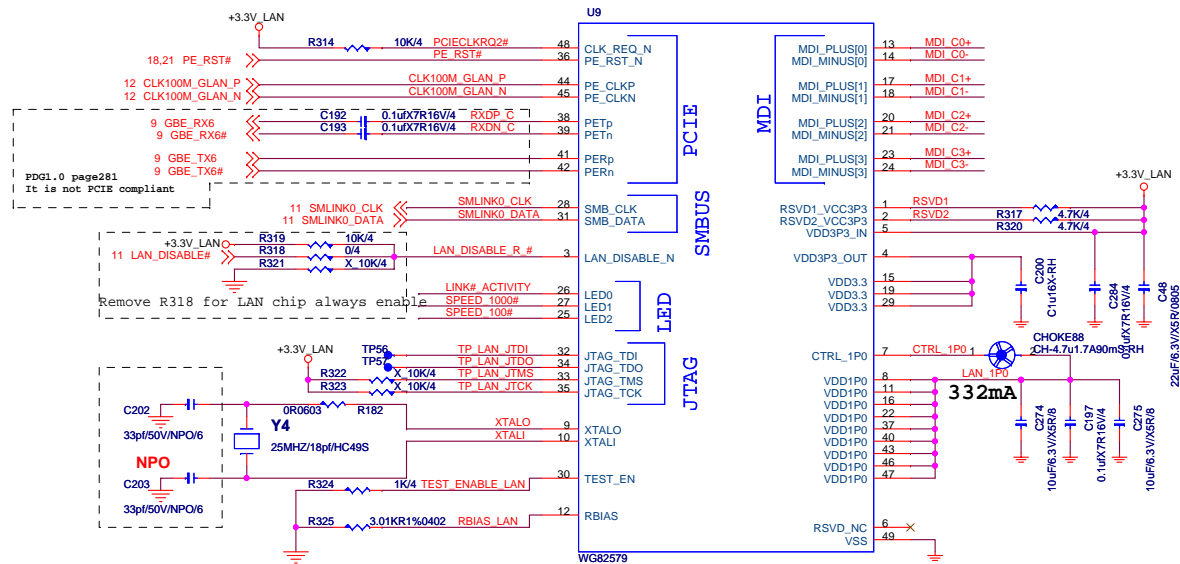
DDPB/C/D_CTRLDATA STRAP

When '1'- Port B is detected; When '0'- Port B is not detected
This signal has a weak internal pull-down.
NOTE: The internal pull-down is disabled after PLTRST# deasserts.

When '1'- Port C is detected; When '0'- Port C is not detected
This signal has a weak internal pull-down.
NOTE: The internal pull-down is disabled after PLTRST# deasserts.

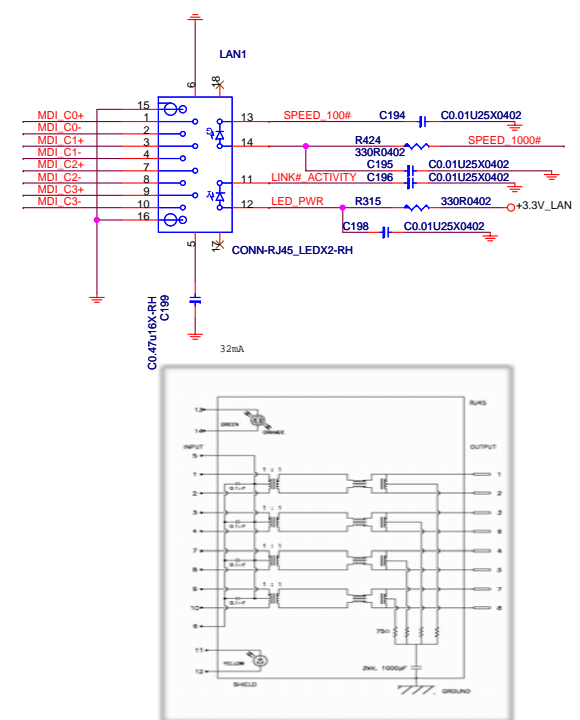
When '1'- Port D is detected; When '0'- Port D is not detected
This signal has a weak internal pull-down.
NOTE: The internal pull-down is disabled after PLTRST# deasserts.

INTEL Lewisville LAN(82579DM)

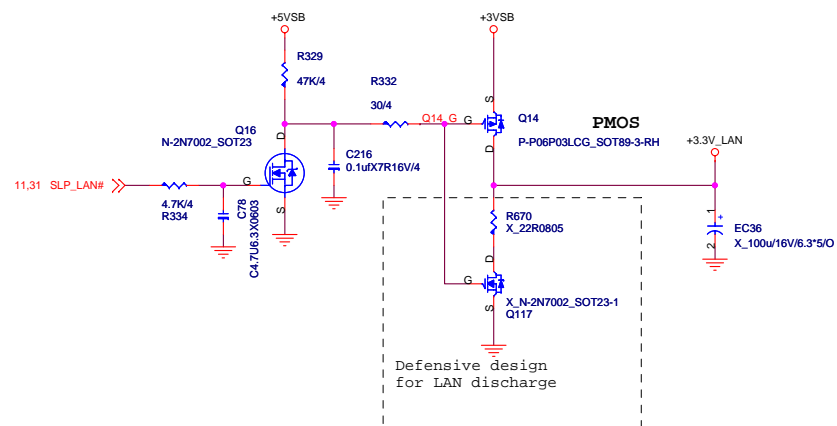


Note that the PHY SMBus address is 0xC8 and default MAC SMBus address is 0xE0.

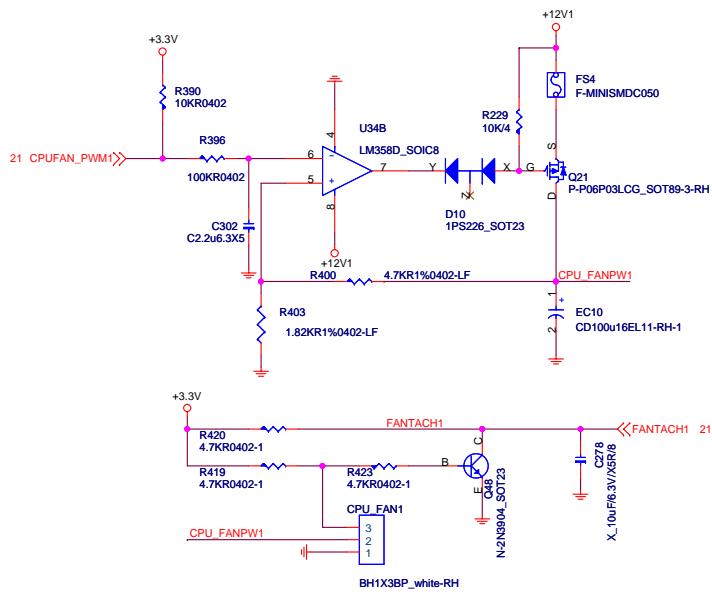
GIGA LAN CONN



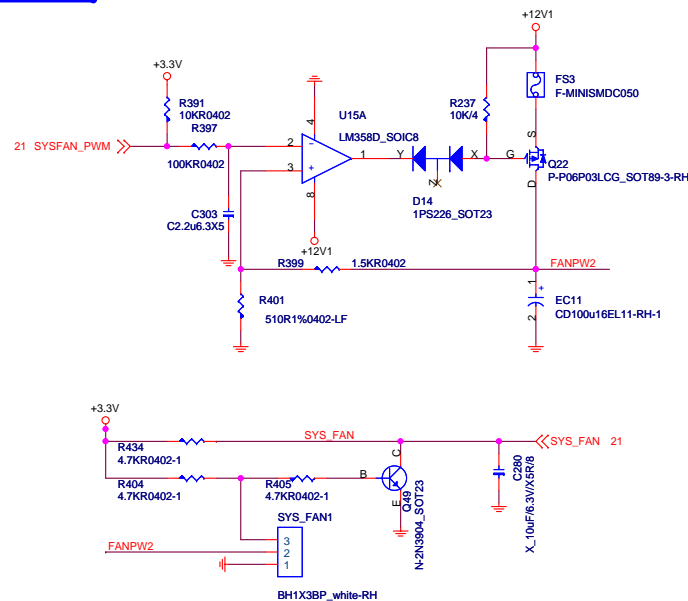
+3.3V LAN
(218mA)



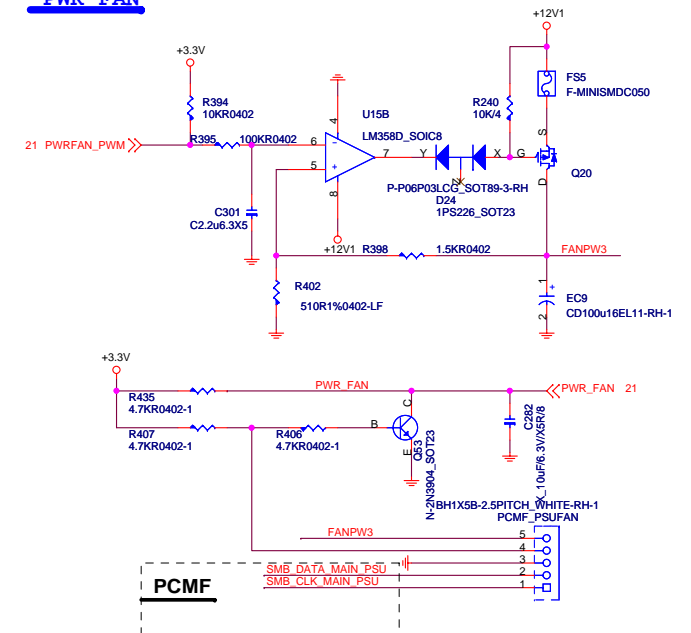
CPU FAN1



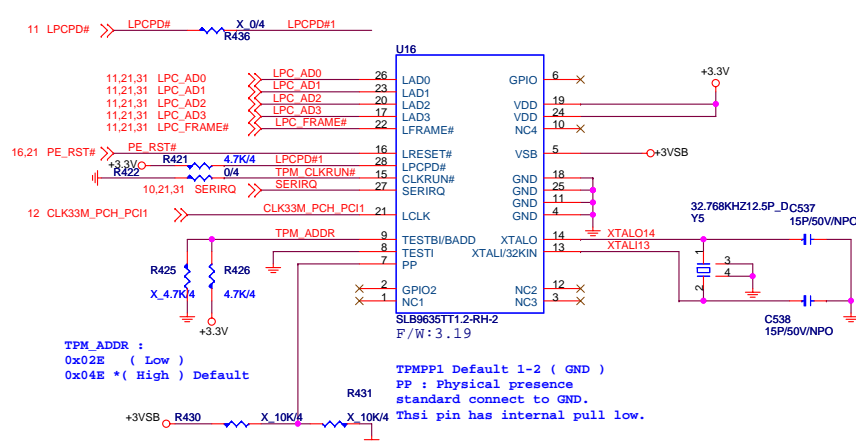
SYS FAN



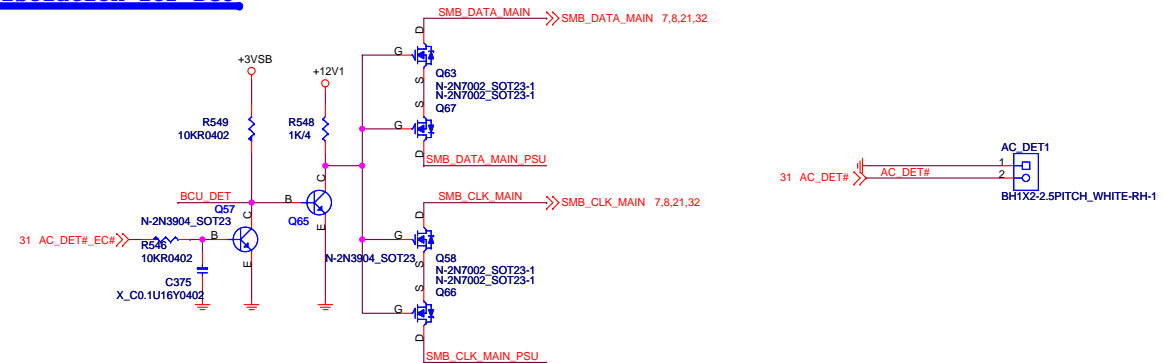
PWR FAN



TPM 1.2



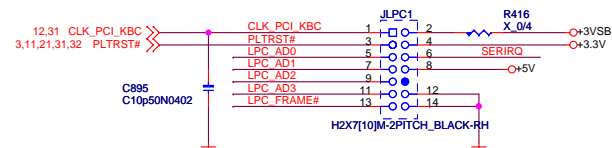
PCMF isolation for BCU



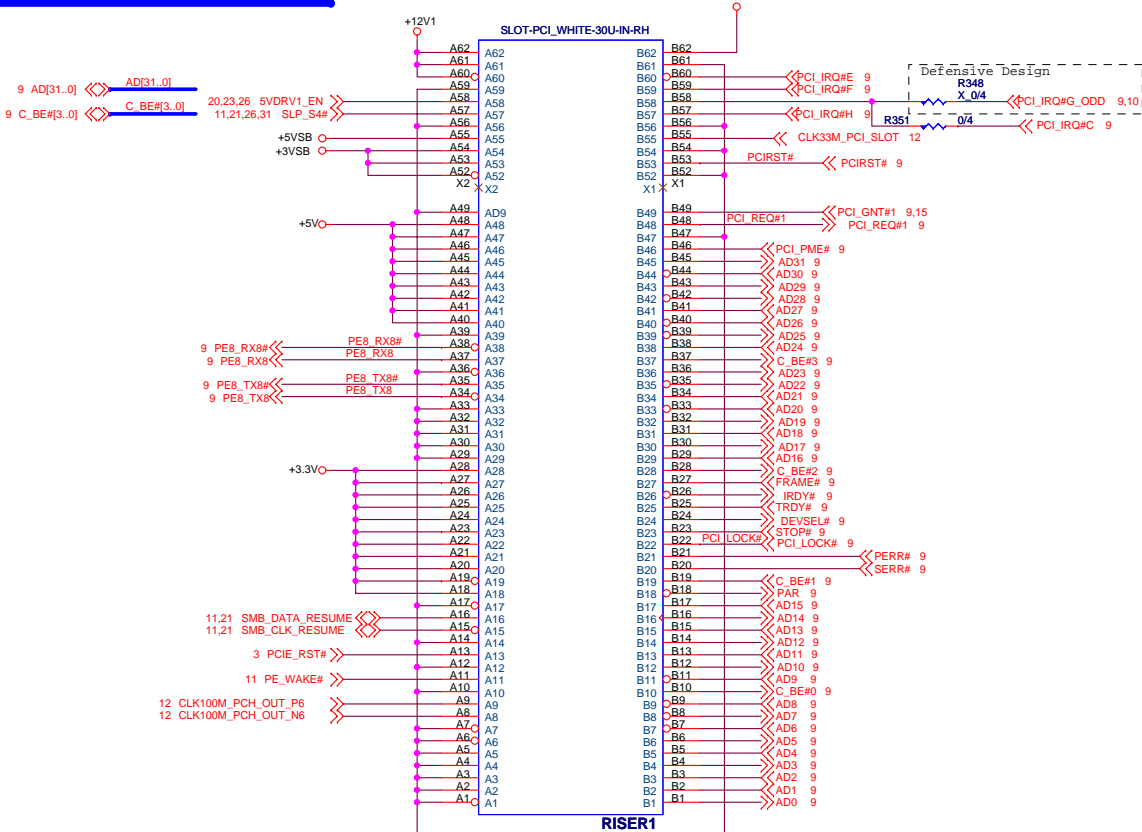
JTPM/80 PORT FOR DEBUG

This connector support

1. debug card (TL309 Rev.1.0)
2. TPM card (MS-4136 Rev.1.0)

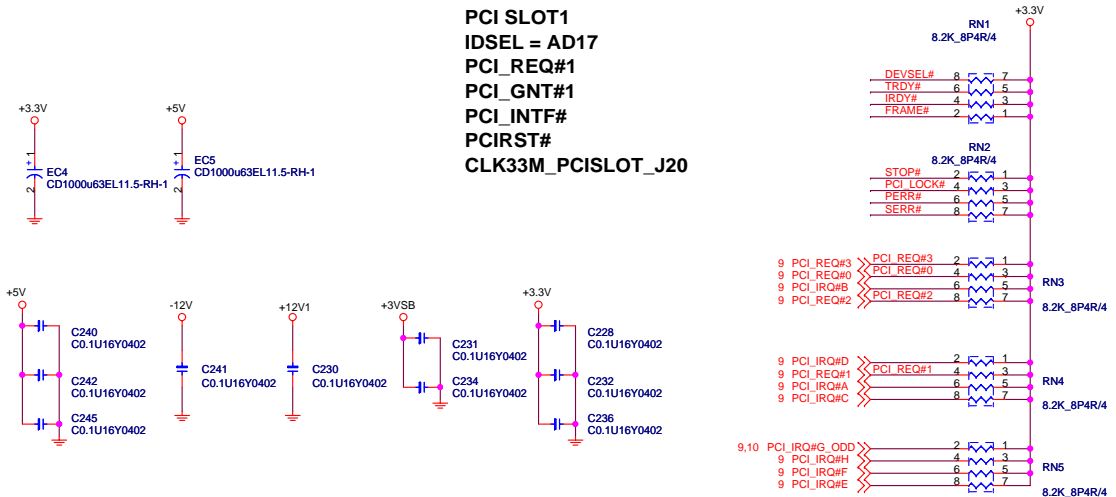


LN riser card interface

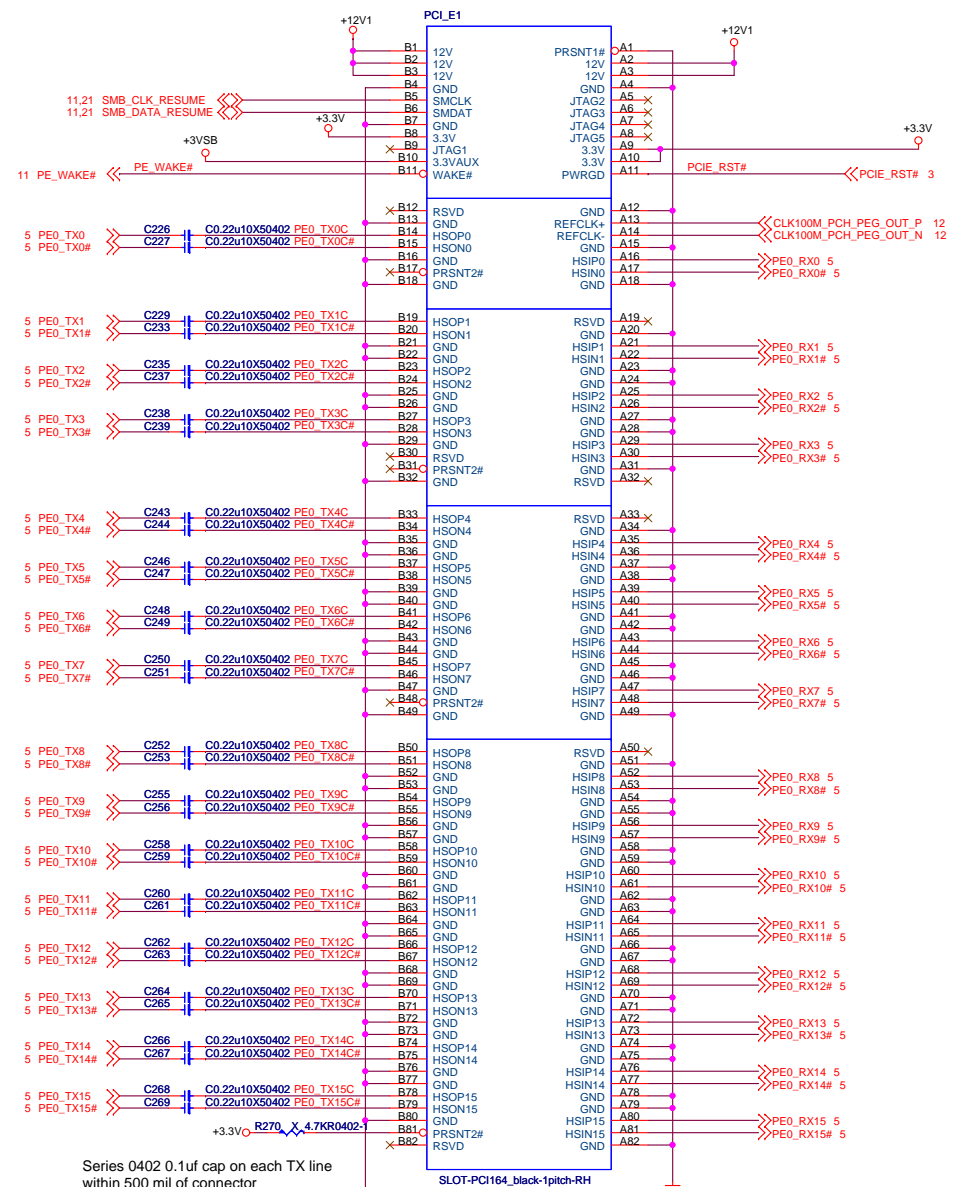


Series 0402 0.1uf cap on each TX line
within 500 mil of connector

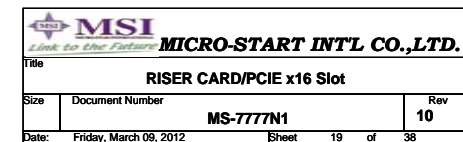
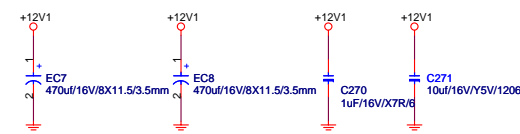
PCI SLOT DECOUPLING CAPS

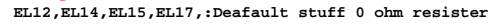


PCIE X16 SLOT

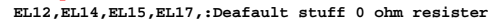
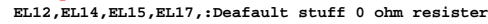


Series 0402 0.1uf cap on each TX line
within 500 mil of connector

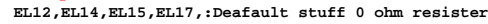


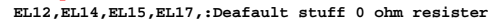
$(1.5A > 800mA)$ 

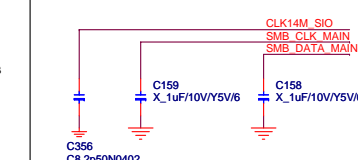
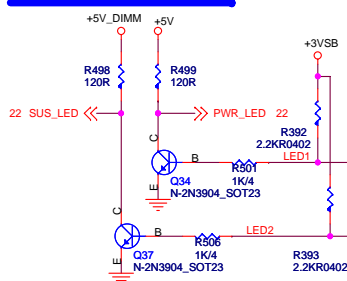
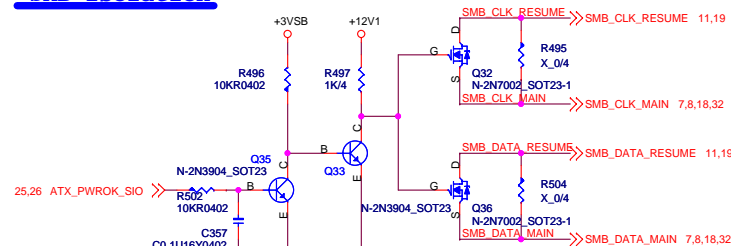
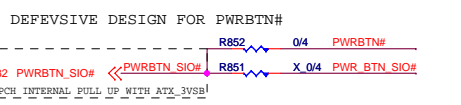
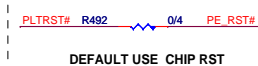
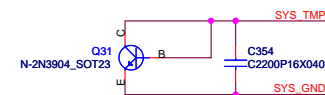
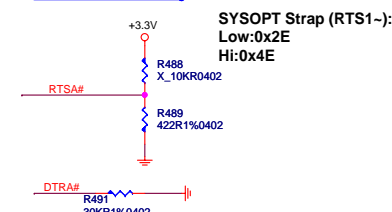
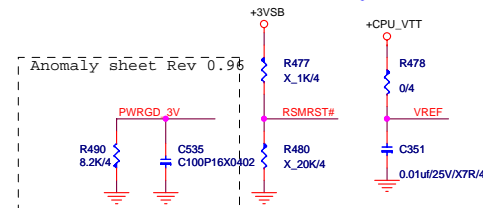
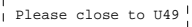
(1.5A>800mA)

 $(1.5A > 1A)$ 

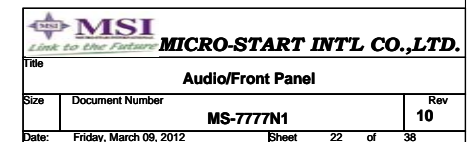
(PORT4-->1.5A>500mA)



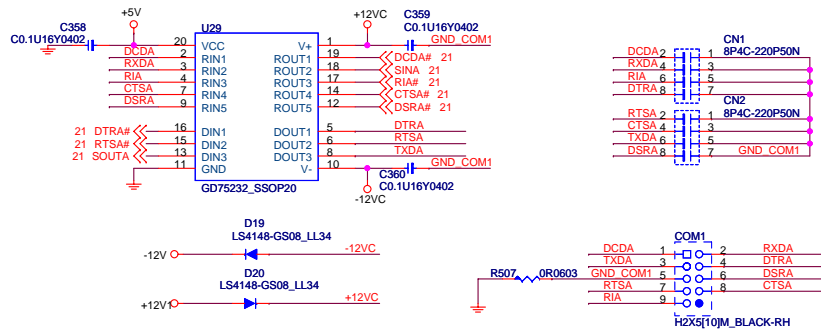




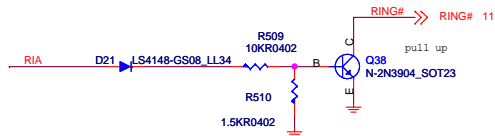
PHONE JACK



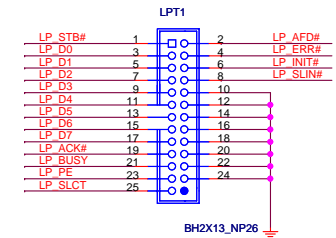
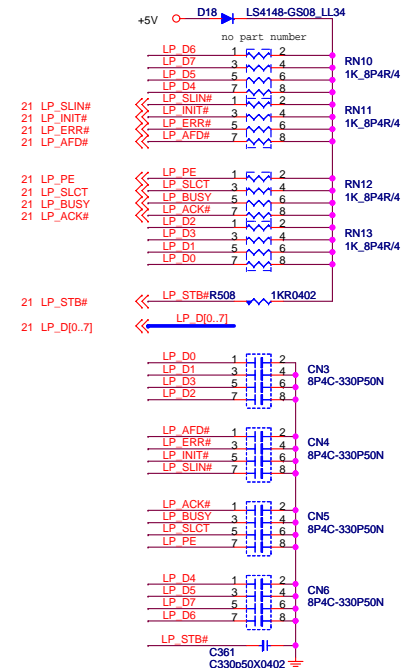
SERIAL PORT



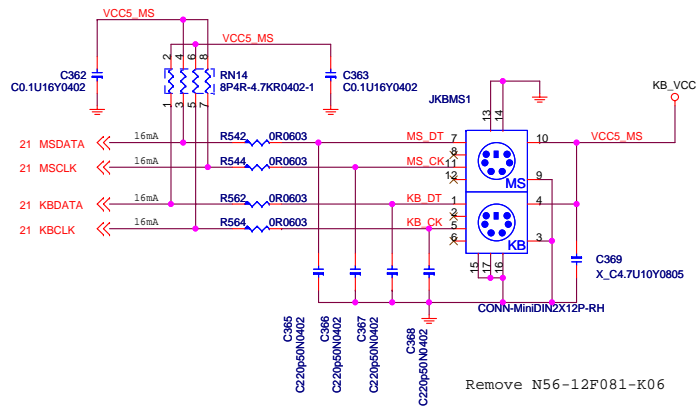
Wake On Modem Header



PARALLAL PORT

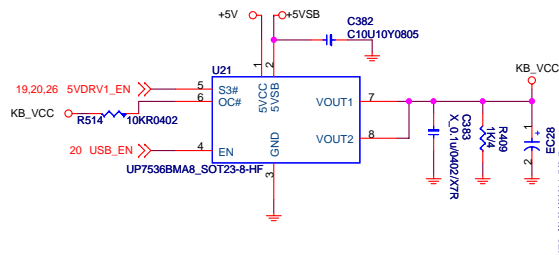


PS2 KEYBOARD & MOUSE CONNECTOR



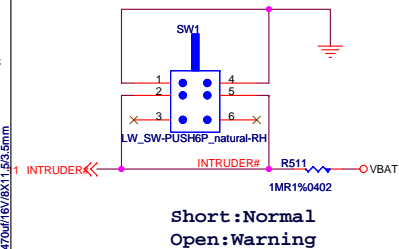
KB/MS POWER

(1.5A > 300mA)

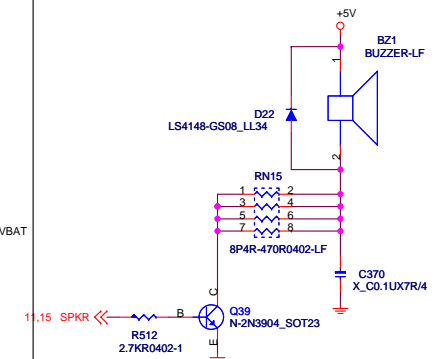


INTRUDER

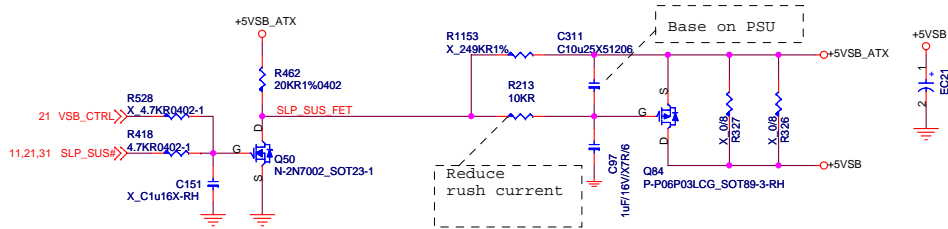
INTRUDER



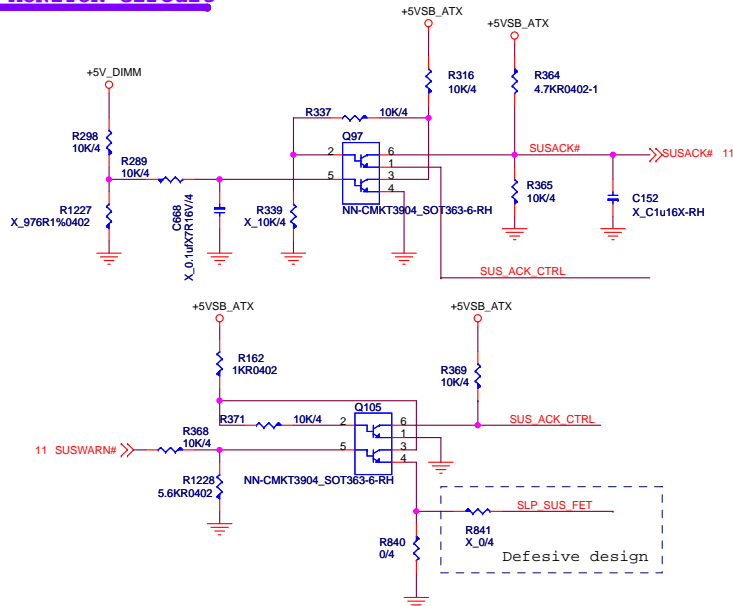
Buzzer



DSW POWER CONTROL CIRCUIT

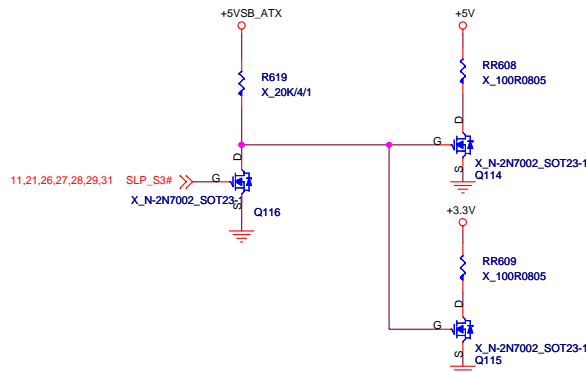


5VDIMM MONITOR Circuit



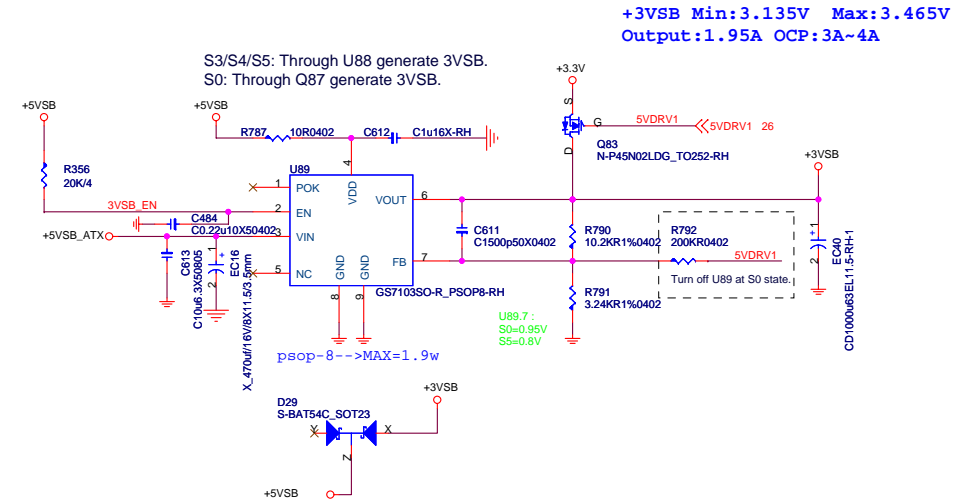
5V/3V Power discharge

DEVEISIVE DESIGN

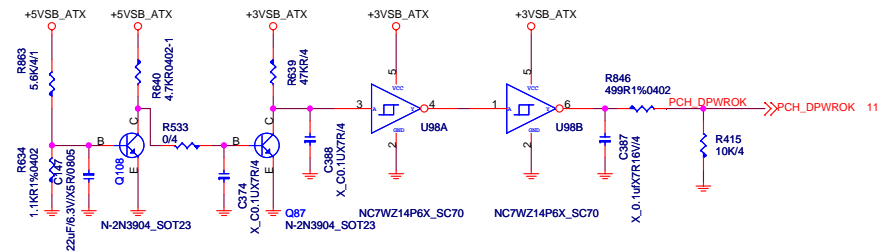


3VSB

(S0=1.5A;S3~S5=0.45A)



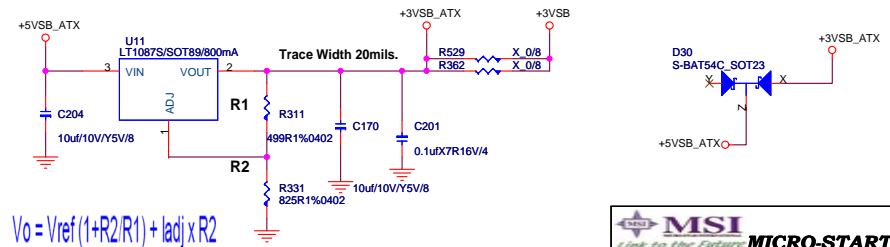
PCH DPWROK CIRCUIT



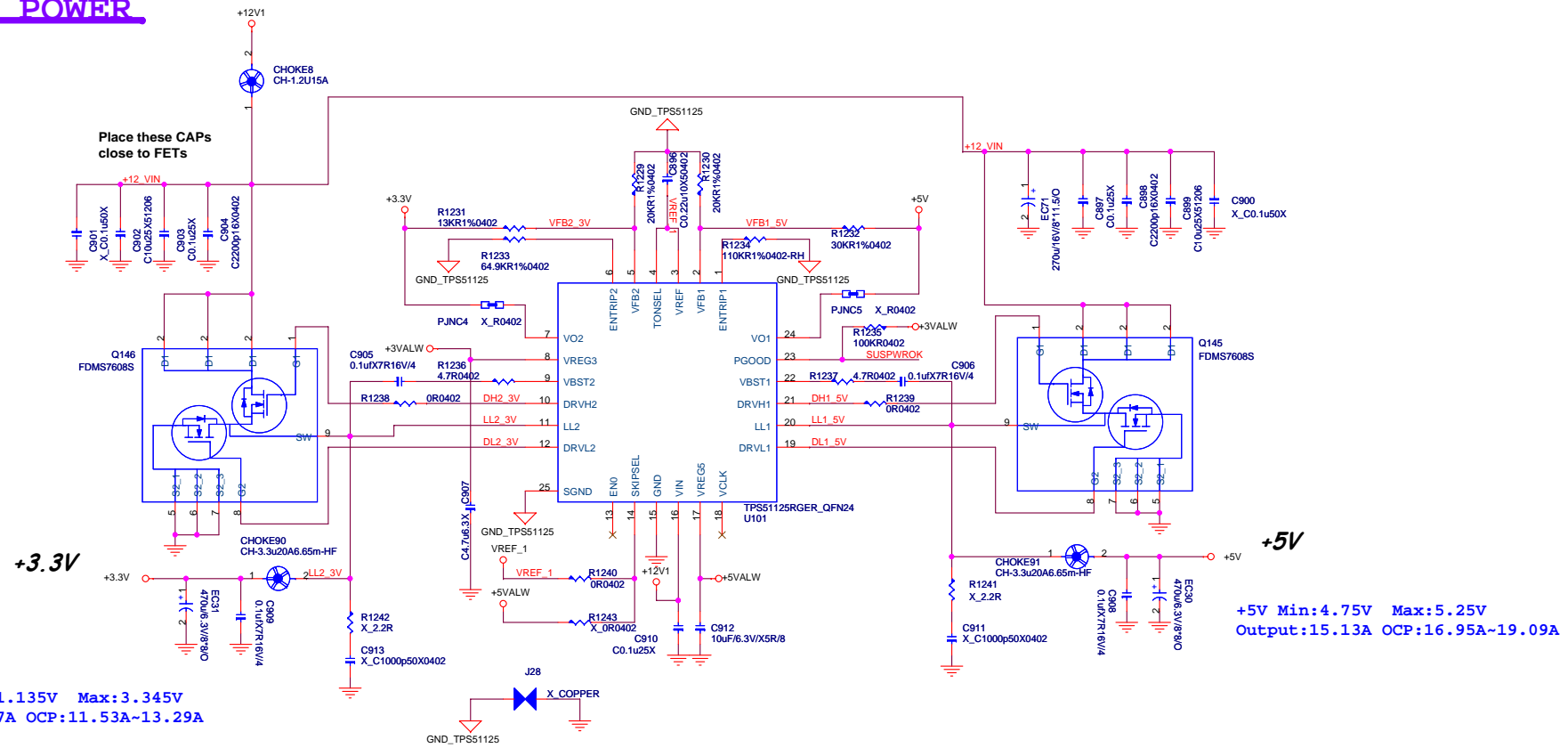
ATX 3VSB

5~10mA

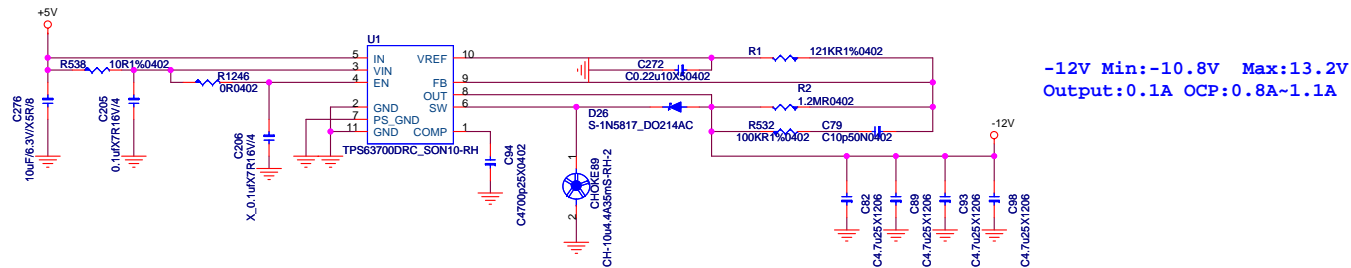
+3VSB_ATX Min:3.135V Max:3.465V
Output:3mA OCP:0.9A~1.2A



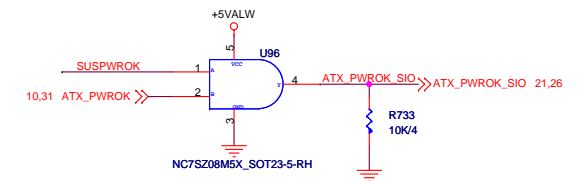
SYSTEM POWER



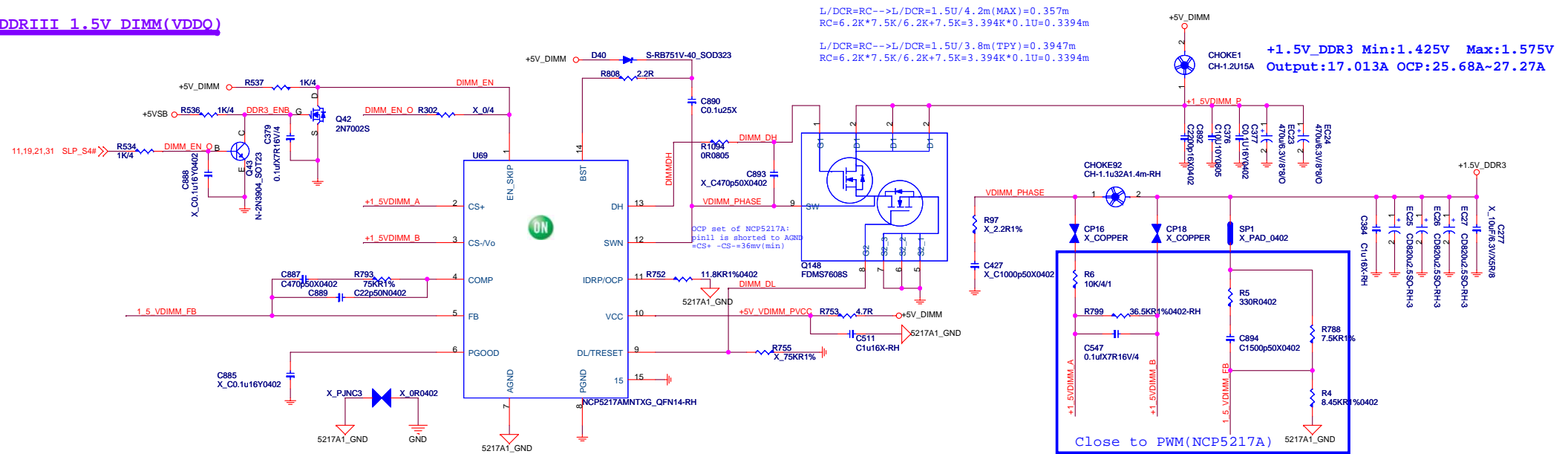
-12V POWER



ATXPWROK Sequency



DDRIII 1.5V DIMM(VDDQ)

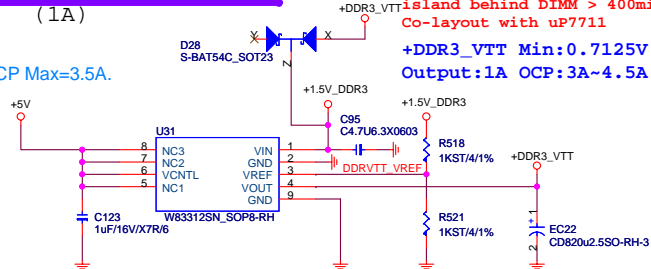


DDR VTT 0.75V Power(VDD IQ)

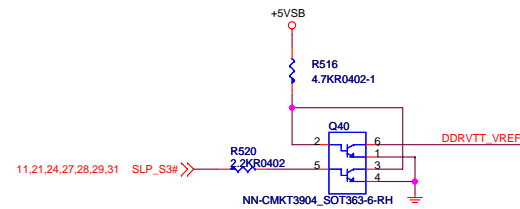
(1A)

To CPU Copper trace width > 250mils , Fill
 island behind DIMM > 400mils .
 Co-layout with uP7711
+DDR3_VTT Min:0.7125V Max:0.7875V
Output:1A OCP:3A-4.5A

VDD_IQ : OCP Max=3.5A.

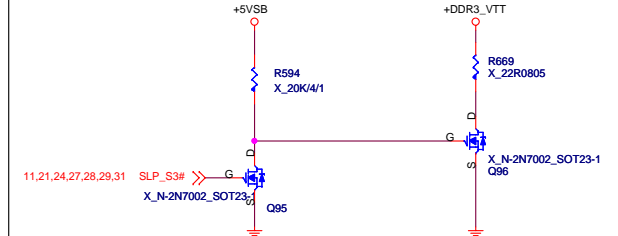


DDR VTT Power Control

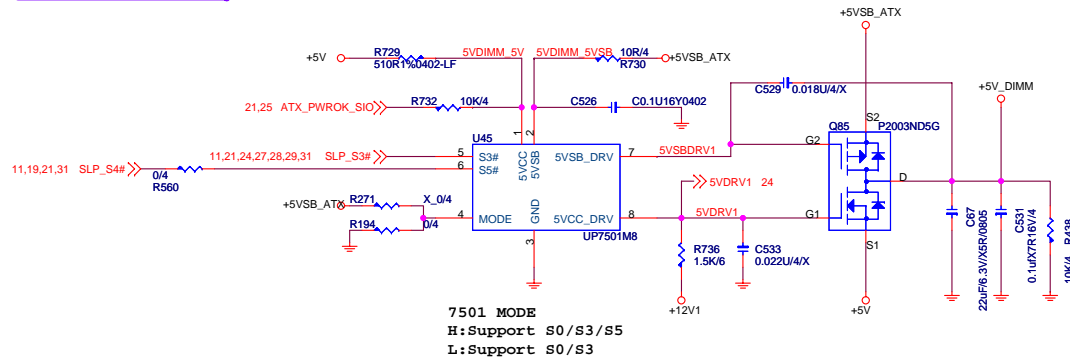


DDR/VTT Power discharge

Defensive design



5VDIMM FOR DDR



PCH MEPWROK

+1.05V_ME
+3VSB
+3VSB

R713 30.1K/4/1
R714 33K/4/1
R711 5.6K/4/1
Q82
C512 0.1uX7R16V/4
C515 C100P50N
R718 301K/4/1
NN-CMKT3904_SOT363-6-RH

+3.3V ME
0.016A

+3VSB
+3.3V_SPI
None AMT Stuff
Q69
X_P-P4402FAG_TSOP6-RH
PMOS
R712 X_0/8
R715 X_10K/4
C621 X_0.1uX7R16V/4
C622 X_C100P50N
C543 X_0.1uX7R16V/4
11 SLP_A PCH_R R611 10K/4
NN-CMKT3904_SOT363-6-RH

ME Power Control

EN 1.05VME
Q70 N-2N7002_SOT23-1
C513 X_C0.1uX7R/4
R717 10K/4
11 SLP_A

+1.05V ME(VCCIO ME)

+1.05V_ME Min:1.045V Max:1.055V
Output:1.61A OCP:4.9A~6A

R720 20K/4
R722 20K/4
C517 C1u16X-RH
PCH MEPWROK R723 X_0/4
R724 4.7/6
C518 C1u16X-RH
VDD U2
C523 C10U10Y0805
C521 22uF/6.3V/X5R/0805
C522
R727 0/4
22uF/6.3V/X5R/0805
U43 ISL8014AIRZ_QFN16-RH
PG U2
R721 10K/4
+3VSB
EN 1.05VME U2
VFB
GND
1.05VME FB
Let ISL8014 go skip mode when power off.
BOTTOM PAD CONNECT TO GND Through 4 VIAs
CONNECT TO GND Through 4 VIAs
CHOKE13 CH-1.2U15A
R725 2.2/8
C524 47p/50V/NPO/4
C525 C1000P16X0402
R726 10K/4/1%
R728 32.4K/4/1%
EC15 470uF/16V/8X11.5S3mm
C519 22uF/6.3V/X5R/0805
C520 22uF/6.3V/X5R/0805
+1.05V_ME
+1.05V
None AMT Stuff
RN20 X_OR/4/8P4R

+1.8V POWER(VCCPLL)

+1.8V Min:1.71V Max:1.89V
Output:1.6A

+3.3V
+12V1
+3.3V
R535 15KR/402/1%
R536 12.1KR/402/1%
C390 C2.2u6.3X5
V1 8SET
R541 1KST/4
R543 X_3KR1%0402
C391 X_C0.1uX7R/4
U34A LM358D_SOIC8
R540 100K/4
Q47 N-P45N02LDG_TO252-RH
EC29 CD1000u63EL11.5-RH-1
C478 C4.7U10Y0805
C532 C0.1U16Y0402
C83 22uF/6.3V/X5R/0805

PCH 1.05V Power Control

PCH 1.05V Power(VCCIO PCH)

+1.05V Min:0.9975V Max:1.1025V
Output:6.2A

+5VSB
+3VSB
+12V1
+1.5V_DDR3
+1.05V
R586 10K/4/1
R587 16.5KR1%
R588 10K/4
R589 7.68KR1%0402-RH
Q51 NN-CMKT3904_SOT363-6-RH
V1P05PCH_CNTRL_INPUT
C410 C2.2u6.3X5
C411 C0.1uX7R/4
C412 X_100p/50V/06
U92A LM358D_SOIC8
R591 1KST/4
R590 100K/4
C438 C0.1U16Y0402
C413 X_C0.1uX7R/4
EC32 CD1000u63EL11.5-RH-1
Q79 N-P45N02LDG_TO252-RH

+CPU VCCP Output caps

+CPU_VCCP

EC44 1+ 1- CD820u2.5SO-RH-3
EC45 1+ 1- CD820u2.5SO-RH-3
EC46 1+ 1- CD820u2.5SO-RH-3
EC47 1+ 1- CD820u2.5SO-RH-3
EC49 1+ 1- CD820u2.5SO-RH-3
EC50 1+ 1- CD820u2.5SO-RH-3
EC51 1+ 1- CD820u2.5SO-RH-3
EC52 1+ 1- CD820u2.5SO-RH-3

SP Capacitors

+CPU_VCCP

EC55 100u/2V/7.3*4.3
EC56 100u/2V/7.3*4.3

+CPU GFX Output caps

+CPU_GFX

EC58 CD620u2.5SO-RH-3
EC59 CD620u2.5SO-RH-3
EC60 CD620u2.5SO-RH-3
EC61 CD620u2.5SO-RH-3
EC62 CD620u2.5SO-RH-3

MSI
Link to the Future
MICRO-START INTL CO.,LTD.

Title: **+1.05V_ME/+3.3V_ME/+1.05V/+1.8V**

Size: Document Number: **MS-7777N1** Rev: **10**

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PCH MEPWROK

+1.05V_ME
+3VSB
+3VSB
R713 30.1K/4/1
R714 33K/4/1
R711 5.6K/4/1
Q82
C512 0.1uX7R16V/4
C515 C100P50N
R718 301K/4/1
NN-CMKT3904_SOT363-6-RH

+3.3V ME
0.016A
+3VSB
R614 10K/4/1
Q86
C621 X_0.1uX7R16V/4
C622 X_C100P50N
C643 X_0.1uX7R16V/4
11 SLP_A8_PCH_R
R611 10K/4
NN-CMKT3904_SOT363-6-RH

ME Power Control
+3VSB
+3.3V_SPI
None AMT Stuff
R712 X_0/8
Q69
X_P-P4402FAG_TSOP6-RH
R850 0/8
+3.3V_LAN
11 SLP_A
R717 10K/4
Q57 B
C513 X_C0.1uX7R/4
Q70 N-2N7002_SOT23-1
EN_1.05VME

+1.05V ME(VCCIO ME)
+3VSB
R720 20K/4
R722 20K/4
C517 C1u16X-RH
PCH MEPWROK R723 X_0/4
R724 4.7/6
C518 C1u16X-RH
C521 22uF/6.3V/X5R/0805
C522
C523 C10U10Y0805
SYMCH
R727 0/4
22uF/6.3V/X5R/0805
EN_1.05VME
PG_U2 R721 10K/4
+3VSB
U43 ISL8014AIRZ_QFN16-RH
EN 5
PG 7
VDD_U2 3
VDD 14
NC2 16
LX1 15
LX2 14
NC1 13
VIN1 2
VIN2 1
SYNCH 4
VFB 8
GND 17
PGND 12
PGND 11
SGND 10
SGND 9
1.05VME_FB
Let ISL8014 go skip mode when power off.
BOTTOM PAD CONNECT TO GND Through 4 VIAs
CONNECT TO GND Through 4 VIAs
CHOKE13 CH-1.2U15A
C524 47p/50V/NPO/4
R725 2.2/8
C525 C1000P16X0402
R726 10K/4/1%
R728 32.4K/4/1%
EC15 470uF/16V/8X11.5-3.5mm
C519 22uF/6.3V/X5R/0805
C520 22uF/6.3V/X5R/0805
RN20 X_OR/4/8P4R
+1.05V_ME
+1.05V
None AMT Stuff

+1.8V POWER(VCCPLL)
+1.8V Min:1.71V Max:1.89V
Output:1.6A
+3.3V
R535 15K/0402/1%
R536 12.1K/0402/1%
C390 C2.2u6.3X5
V1 8SET
R541 1KST/4
R543 X_3KR1%0402
C391 X_C0.1uX7R/4
U34A LM358D_SOIC8
R540 100K/4
Q47 N-P45N02LDG_TO252-RH
CD1000u63EL11.5-RH-1
EC29
+12V1
+3.3V
C83 22uF/6.3V/X5R/0805
C532 C0.1U16Y0402
C478 C4.7U10Y0805

PCH 1.05V Power Control
+5VSB
R586 10K/4/1
R587 16.5KR1%
V1P05PCH_CNTRL_INPUT
Q51
NN-CMKT3904_SOT363-6-RH
R588 10K/4
C411 C0.1uX7R/4
C410 C2.2u6.3X5
R589 7.68KR1%0402-RH
U92A LM358D_SOIC8
R591 1KST/4
C412 X_100p/50V/06
C413 X_C0.1uX7R/4
EC32 CD1000u63EL11.5-RH-1
R590 100K/4
+1.5V_DDR3
+1.05V

PCH 1.05V Power(VCCIO PCH)
+1.05V Min:0.9975V Max:1.1025V
Output:6.2A
+12V1
+1.5V_DDR3
+1.05V

+CPU VCCP Output caps
+CPU_VCCP
EC44 1+ 100u/2V/7.3*4.3
EC45 1+ 100u/2V/7.3*4.3
EC46 1+ 100u/2V/7.3*4.3
EC47 1+ 100u/2V/7.3*4.3
EC49 1+ 100u/2V/7.3*4.3
EC50 1+ 100u/2V/7.3*4.3
EC51 1+ 100u/2V/7.3*4.3
EC52 1+ 100u/2V/7.3*4.3

SP Capacitors
+CPU_VCCP
EC55 100u/2V/7.3*4.3
EC56 100u/2V/7.3*4.3

+CPU GFX Output caps
+CPU_GFX
EC58 100u/2V/7.3*4.3
EC59 100u/2V/7.3*4.3
EC60 100u/2V/7.3*4.3
EC61 100u/2V/7.3*4.3
EC62 100u/2V/7.3*4.3

MSI MICRO-START INTL CO.,LTD.
Title: +1.05V_ME/+3.3V_ME/+1.05V/+1.8V
Size: Document Number
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Date: Friday, March 09, 2012
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PCH MEPWROK

+1.05V_ME
+3VSB
+3VSB

R713 30.1K/4/1
R714 33K/4/1
R711 5.6K/4/1
Q82
C512 0.1uX7R16V/4
C515 C100P50N
R718 301K/4/1
NN-CMKT3904_SOT363-6-RH

+3.3V ME
0.016A

+3VSB
+3.3V_SPI
None AMT Stuff
Q69
X_P-P4402FAG_TSOP6-RH
PMOS
R712 X_0/8
R715 X_10K/4
C621 X_0.1uX7R16V/4
C622 X_C100P50N
C543 X_0.1uX7R16V/4
11 SLP_A PCH_R R611 10K/4
NN-CMKT3904_SOT363-6-RH

ME Power Control

EN 1.05VME
Q70 N-2N7002_SOT23-1
C513 X_C0.1uX7R/4
R717 10K/4
11 SLP_A

+1.05V ME(VCCIO ME)

+1.05V_ME Min:1.045V Max:1.055V
Output:1.61A OCP:4.9A~6A

R720 20K/4
R722 20K/4
C517 C1u16X-RH
PCH MEPWROK R723 X_0/4
R724 4.7/6
C518 C1u16X-RH
VDD U2
C523 C10U10Y0805
C521 22uF/6.3V/X5R/0805
C522
R727 0/4
22uF/6.3V/X5R/0805
U43 ISL8014AIRZ_QFN16-RH
PG U2
R721 10K/4
+3VSB
EN 1.05VME U2
VFB
GND
1.05VME FB
Let ISL8014 go skip mode when power off.
BOTTOM PAD CONNECT TO GND Through 4 VIAs
CONNECT TO GND Through 4 VIAs
CHOKE13 CH-1.2U15A
R725 2.2/8
C524 47p/50V/NPO/4
C525 C1000P16X0402
R726 10K/4/1%
R728 32.4K/4/1%
EC15 470uF/16V/8X11.5S3mm
C519 22uF/6.3V/X5R/0805
C520 22uF/6.3V/X5R/0805
+1.05V_ME
+1.05V
None AMT Stuff
RN20 X_OR/4/8P4R

+1.8V POWER(VCCPLL)

+1.8V Min:1.71V Max:1.89V
Output:1.6A

+3.3V
+12V1
+3.3V
R535 15KR/402/1%
R536 12.1KR/402/1%
C390 C2.2u6.3X5
V1 8SET
R541 1KST/4
R543 X_3KR1%0402
C391 X_C0.1uX7R/4
U34A LM358D_SOIC8
R540 100K/4
Q47 N-P45N02LDG_TO252-RH
CD1000u63EL11.5-RH-1
EC29
C478 C4.7U10Y0805
C532 C0.1U16Y0402
C83 22uF/6.3V/X5R/0805

PCH 1.05V Power Control

PCH 1.05V Power(VCCIO PCH)

+1.05V Min:0.9975V Max:1.1025V
Output:6.2A

+5VSB
+3VSB
+12V1
+1.5V_DDR3
+1.05V
R586 10K/4/1
R587 16.5KR1%
R588 10K/4
R589 7.68KR1%0402-RH
Q51 NN-CMKT3904_SOT363-6-RH
V1P05PCH_CNTRL_INPUT
C410 C2.2u6.3X5
C411 C0.1uX7R/4
C412 X_100p/50V/06
U92A LM358D_SOIC8
R591 1KST/4
R590 100K/4
C438 C0.1U16Y0402
C413 X_C0.1uX7R/4
EC32 CD1000u63EL11.5-RH-1
Q79 N-P45N02LDG_TO252-RH

+CPU VCCP Output caps

+CPU_VCCP

EC44 1+ 100u/2V/7.3*4.3
EC45 1+ 100u/2V/7.3*4.3
EC46 1+ 100u/2V/7.3*4.3
EC47 1+ 100u/2V/7.3*4.3
EC49 1+ 100u/2V/7.3*4.3
EC50 1+ 100u/2V/7.3*4.3
EC51 1+ 100u/2V/7.3*4.3
EC52 1+ 100u/2V/7.3*4.3

SP Capacitors

+CPU_VCCP

EC55 100u/2V/7.3*4.3
EC56 100u/2V/7.3*4.3

+CPU GFX Output caps

+CPU_GFX

EC58 100u/2V/7.3*4.3
EC59 100u/2V/7.3*4.3
EC60 100u/2V/7.3*4.3
EC61 100u/2V/7.3*4.3
EC62 100u/2V/7.3*4.3

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Title: **+1.05V_ME/+3.3V_ME/+1.05V/+1.8V**

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PCH MEPWROK

+1.05V_ME
+3VSB
+3VSB

R713 30.1K/4/1
R714 33K/4/1
R711 5.6K/4/1
Q82
C512 0.1uX7R16V/4
C515 C100P50N
R718 301K/4/1
NN-CMKT3904_SOT363-6-RH

+3.3V ME
0.016A

+3VSB
+3.3V_SPI
None AMT Stuff
Q69
X_P-P4402FAG_TSOP6-RH
PMOS
R712 X_0/8
R715 X_10K/4
C621 X_0.1uX7R16V/4
C622 X_C100P50N
C543 X_0.1uX7R16V/4
11 SLP_A PCH_R R611 10K/4
NN-CMKT3904_SOT363-6-RH

ME Power Control

EN 1.05VME
Q70 N-2N7002_SOT23-1
C513 X_C0.1uX7R/4
R717 10K/4
11 SLP_A

+1.05V ME(VCCIO ME)

+1.05V_ME Min:1.045V Max:1.055V
Output:1.61A OCP:4.9A~6A

R720 20K/4
R722 20K/4
C517 C1u16X-RH
PCH MEPWROK R723 X_0/4
R724 4.7/6
C518 C1u16X-RH
VDD U2
C523 C10U10Y0805
C521 22uF/6.3V/X5R/0805
C522
R727 0/4
22uF/6.3V/X5R/0805
U43 ISL8014AIRZ_QFN16-RH
PG U2
R721 10K/4
+3VSB
EN 1.05VME U2
VFB
GND
1.05VME_FB
Let ISL8014 go skip mode when power off.
BOTTOM PAD CONNECT TO GND Through 4 VIAs
CONNECT TO GND Through 4 VIAs
CHOKE13 CH-1.2U15A
R725 2.2/8
C524 47p/50V/NPO/4
C525 C1000P16X0402
R726 10K/4/1%
R728 32.4K/4/1%
EC15 470uF/16V/8X11.5S3mm
C519 22uF/6.3V/X5R/0805
C520 22uF/6.3V/X5R/0805
RN20 X_OR/4/8P4R
+1.05V_ME
+1.05V
None AMT Stuff

+1.8V POWER(VCCPLL)

+1.8V Min:1.71V Max:1.89V
Output:1.6A

+3.3V
+12V1
+3.3V
R535 15KR/402/1%
R536 12.1KR/402/1%
C390 C2.2u6.3X5
V1 8SET
R541 1KST/4
R543 X_3KR1%0402
C391 X_C0.1uX7R/4
U34A LM358D_SOIC8
R540 100K/4
Q47 N-P45N02LDG_TO252-RH
EC29 CD1000u63EL11.5-RH-1
C478 C4.7U10Y0805
C532 C0.1U16Y0402
C83 22uF/6.3V/X5R/0805

PCH 1.05V Power Control

PCH 1.05V Power(VCCIO PCH)

+1.05V Min:0.9975V Max:1.1025V
Output:6.2A

+5VSB
+3VSB
+12V1
+1.5V_DDR3
+1.05V
R586 10K/4/1
R587 16.5KR1%
R588 10K/4
R589 7.68KR1%0402-RH
Q51 NN-CMKT3904_SOT363-6-RH
V1P05PCH_CNTRL_INPUT
C410 C2.2u6.3X5
C411 C0.1uX7R/4
C412 X_100p/50V/06
U92A LM358D_SOIC8
R591 1KST/4
R590 100K/4
C438 C0.1U16Y0402
C439 105G
Q79 N-P45N02LDG_TO252-RH
EC32 CD1000u63EL11.5-RH-1
C413 X_C0.1uX7R/4

+CPU VCCP Output caps

+CPU_VCCP

EC44 1+ 1- CD820u2.5SO-RH-3
EC45 1+ 1- CD820u2.5SO-RH-3
EC46 1+ 1- CD820u2.5SO-RH-3
EC47 1+ 1- CD820u2.5SO-RH-3
EC49 1+ 1- CD820u2.5SO-RH-3
EC50 1+ 1- CD820u2.5SO-RH-3
EC51 1+ 1- CD820u2.5SO-RH-3
EC52 1+ 1- CD820u2.5SO-RH-3

SP Capacitors

+CPU_VCCP

EC55 100u/2V/7.3*4.3
EC56 100u/2V/7.3*4.3

+CPU GFX Output caps

+CPU_GFX

EC58 CD620u2.5SO-RH-3
EC59 CD620u2.5SO-RH-3
EC60 CD620u2.5SO-RH-3
EC61 CD620u2.5SO-RH-3
EC62 CD620u2.5SO-RH-3

MSI
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MICRO-START INTL CO.,LTD.

Title: **+1.05V_ME/+3.3V_ME/+1.05V/+1.8V**

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PCH MEPWROK

+1.05V_ME
+3VSB
+3VSB
R713 30.1K/4/1
R714 33K/4/1
R711 5.6K/4/1
Q82
C512 0.1uX7R16V/4
C515 C100P50N
R718 301K/4/1
NN-CMKT3904_SOT363-6-RH

+3.3V ME
0.016A
+3VSB
R614 10K/4/1
Q86
C621 X_0.1uX7R16V/4
C622 X_C100P50N
C643 X_0.1uX7R16V/4
11 SLP_A8_PCH_R
R611 10K/4
NN-CMKT3904_SOT363-6-RH

ME Power Control
+3VSB
+3.3V_SPI
None AMT Stuff
R712 X_0/8
Q69
X_P-P4402FAG_TSOP6-RH
R850 0/8
+3.3V_LAN
11 SLP_A
R717 10K/4
Q57 B
C513 X_C0.1uX7R/4
Q70 N-2N7002_SOT23-1
EN_1.05VME

+1.05V ME(VCCIO ME)
+3VSB
R720 20K/4
R722 20K/4
C517 C1u16X-RH
PCH MEPWROK R723 X_0/4
R724 4.7/6
C518 C1u16X-RH
C521 22uF/6.3V/X5R/0805
C522
C523 C10U10Y0805
SYMCH
R727 0/4
22uF/6.3V/X5R/0805
EN_1.05VME
PG_U2 R721 10K/4
+3VSB
U43 ISL8014AIRZ_QFN16-RH
EN 5
PG 7
VDD_U2 3
VDD 14
NC3 6
VIN1 2
VIN2 1
SYNCH 4
VFB 8
GND 17
PGND 12
SGND 11
NC2 16
LX1 15
LX2 14
NC1 13
1.05VME_U2
CHOKE13 CH-1.2U15A
R725 2.2/8
C524 47p/50V/NPO/4
C525 C1000P16X0402
R726 10K/4/1%
R728 32.4K/4/1%
EC15 470uF/16V/8X11.5S3mm
C519 22uF/6.3V/X5R/0805
C520 22uF/6.3V/X5R/0805
RN20 X_OR/4/8P4R
+1.05V_ME
+1.05V
None AMT Stuff
Let ISL8014 go skip mode when power off.
BOTTOM PAD CONNECT TO GND Through 4 VIAs
CONNECT TO GND Through 4 VIAs

+1.8V POWER(VCCPLL)
+1.8V Min:1.71V Max:1.89V
Output:1.6A
+3.3V
R535 15K/0.402/1%
R536 12.1K/0.402/1%
C390 C2.2u6.3X5
V1 8SET
R541 1KST/4
R543 X_3KR1%0402
C391 X_C0.1uX7R/4
U34A LM358D_SOIC8
R540 100K/4
Q47 N-P45N02LDG_TO252-RH
CD1000u63EL11.5-RH-1
EC29
+12V1
+3.3V
C83 22uF/6.3V/X5R/0805
C532 C0.1U16Y0402
C478 C4.7U10Y0805

PCH 1.05V Power Control
+5VSB
R586 10K/4/1
R587 16.5KR1%
V1P05PCH_CNTRL_INPUT
Q51
NN-CMKT3904_SOT363-6-RH
R588 10K/4
C411 C0.1uX7R/4
C410 C2.2u6.3X5
R589 7.68KR1%0402-RH
U92A LM358D_SOIC8
R591 1KST/4
C412 X_100p/50V/06
C413 X_C0.1uX7R/4
EC32 CD1000u63EL11.5-RH-1
R590 100K/4
+1.5V_DDR3
+1.05V

PCH 1.05V Power(VCCIO PCH)
+1.05V Min:0.9975V Max:1.1025V
Output:6.2A
+1.05V_ME
+1.05V
None AMT Stuff
RN20 X_OR/4/8P4R

+CPU VCCP Output caps
+CPU_VCCP
EC44 1+ 100u/2V/7.3*4.3
EC45 1+ 100u/2V/7.3*4.3
EC46 1+ 100u/2V/7.3*4.3
EC47 1+ 100u/2V/7.3*4.3
EC49 1+ 100u/2V/7.3*4.3
EC50 1+ 100u/2V/7.3*4.3
EC51 1+ 100u/2V/7.3*4.3
EC52 1+ 100u/2V/7.3*4.3

SP Capacitors
+CPU_VCCP
EC55 100u/2V/7.3*4.3
EC56 100u/2V/7.3*4.3

+CPU GFX Output caps
+CPU_GFX
EC58 100u/2V/7.3*4.3
EC59 100u/2V/7.3*4.3
EC60 100u/2V/7.3*4.3
EC61 100u/2V/7.3*4.3
EC62 100u/2V/7.3*4.3

MSI MICRO-START INTL CO.,LTD.
Title: +1.05V_ME/+3.3V_ME/+1.05V/+1.8V
Size: Document Number
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PCH MEPWROK

+1.05V_ME Min:1.045V Max:1.055V
Output:1.61A OCP:4.9A~6A

+3.3V ME
0.016A

ME Power Control

+1.05V ME(VCCIO ME)

+1.8V POWER(VCCPLL)
+1.8V Min:1.71V Max:1.89V
Output:1.6A

PCH 1.05V Power Control

PCH 1.05V Power(VCCIO PCH)
+1.05V Min:0.9975V Max:1.1025V
Output:6.2A

+CPU VCCP Output caps

SP Capacitors

+CPU GFX Output caps

MSI
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MICRO-START INT'L CO.,LTD.

Title	+1.05V_ME/+3.3V_ME/+1.05V/+1.8V		
Size	Document Number	Rev	
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PCH MEPWROK

+1.05V_ME
+3VSB
+3VSB

R713 30.1K/4/1
R714 33K/4/1
R711 5.6K/4/1
Q82
C512 0.1uX7R16V/4
C515 C100P50N
R718 301K/4/1
NN-CMKT3904_SOT363-6-RH

+3.3V ME
0.016A

+3VSB
+3.3V_SPI
None AMT Stuff
Q69
X_P-P4402FAG_TSOP6-RH
PMOS
R712 X_0/8
R715 X_10K/4
C621 X_0.1uX7R16V/4
C622 X_C100P50N
C543 X_0.1uX7R16V/4
11 SLP_A PCH_R R611 10K/4
NN-CMKT3904_SOT363-6-RH

ME Power Control

EN 1.05VME
Q70 N-2N7002_SOT23-1
C513 X_C0.1uX7R/4
R717 10K/4
11 SLP_A

+1.05V ME(VCCIO ME)

+1.05V_ME Min:1.045V Max:1.055V
Output:1.61A OCP:4.9A~6A

R720 20K/4
R722 20K/4
C517 C1u16X-RH
PCH MEPWROK R723 X_0/4
R724 4.7/6
C518 C1u16X-RH
VDD U2
C523 C10U10Y0805
C521 22uF/6.3V/X5R/0805
C522
R727 0/4
22uF/6.3V/X5R/0805
U43 ISL8014AIRZ_QFN16-RH
PG U2
R721 10K/4
+3VSB
EN 1.05VME U2
VFB
GND
1.05VME_FB
Let ISL8014 go skip mode when power off.
BOTTOM PAD CONNECT TO GND Through 4 VIAs
CONNECT TO GND Through 4 VIAs
CHOKE13 CH-1.2U15A
R725 2.2/8
C524 47p/50V/NPO/4
C525 C1000P16X0402
R726 10K/4/1%
R728 32.4K/4/1%
EC15 470uF/16V/8X11.5S3mm
C519 22uF/6.3V/X5R/0805
C520 22uF/6.3V/X5R/0805
RN20 X_OR/4/8P4R
+1.05V_ME
+1.05V
None AMT Stuff

+1.8V POWER(VCCPLL)

+1.8V Min:1.71V Max:1.89V
Output:1.6A

+3.3V
+12V1
+3.3V
R535 15KR/402/1%
R536 12.1KR/402/1%
C390 C2.2u6.3X5
V1 8SET
R541 1KST/4
R543 X_3KR1%0402
C391 X_C0.1uX7R/4
U34A LM358D_SOIC8
R540 100K/4
Q47 N-P45N02LDG_TO252-RH
EC29 CD1000u63EL11.5-RH-1
C478 C4.7U10Y0805
C532 C0.1U16Y0402
C83 22uF/6.3V/X5R/0805

PCH 1.05V Power Control

PCH 1.05V Power(VCCIO PCH)

+1.05V Min:0.9975V Max:1.1025V
Output:6.2A

+5VSB
+3VSB
+12V1
+1.5V_DDR3
+1.05V
R586 10K/4/1
R587 16.5KR1%
R588 10K/4
R589 7.68KR1%0402-RH
Q51 NN-CMKT3904_SOT363-6-RH
V1P05PCH_CNTRL_INPUT
C410 C2.2u6.3X5
C411 C0.1uX7R/4
C412 X_100p/50V/06
U92A LM358D_SOIC8
R591 1KST/4
R590 100K/4
C438 C0.1u16Y0402
C413 X_C0.1uX7R/4
EC32 CD1000u63EL11.5-RH-1
Q79 N-P45N02LDG_TO252-RH

+CPU VCCP Output caps

+CPU_VCCP

EC44 1+ 1- CD820u2.5SO-RH-3
EC45 1+ 1- CD820u2.5SO-RH-3
EC46 1+ 1- CD820u2.5SO-RH-3
EC47 1+ 1- CD820u2.5SO-RH-3
EC49 1+ 1- CD820u2.5SO-RH-3
EC50 1+ 1- CD820u2.5SO-RH-3
EC51 1+ 1- CD820u2.5SO-RH-3
EC52 1+ 1- CD820u2.5SO-RH-3

SP Capacitors

+CPU_VCCP

EC55 100u/2V/7.3*4.3
EC56 100u/2V/7.3*4.3

+CPU GFX Output caps

+CPU_GFX

EC58 CD620u2.5SO-RH-3
EC59 CD620u2.5SO-RH-3
EC60 CD620u2.5SO-RH-3
EC61 CD620u2.5SO-RH-3
EC62 CD620u2.5SO-RH-3

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Title: **+1.05V_ME/+3.3V_ME/+1.05V/+1.8V**

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PCH MEPWROK

+3.3V ME
0.016A

ME Power Control

+1.05V ME (VCCIO ME)

+1.05V ME Min:1.045V Max:1.055V
Output:1.61A OCP:4.9A~6A

+1.8V POWER (VCCPLL)

+1.8V Min:1.71V Max:1.89V
Output:1.6A

PCH 1.05V Power Control

PCH 1.05V Power (VCCIO PCH)

+1.05V Min:0.9975V Max:1.1025V
Output:6.2A

+CPU VCCP Output caps

SP Capacitors

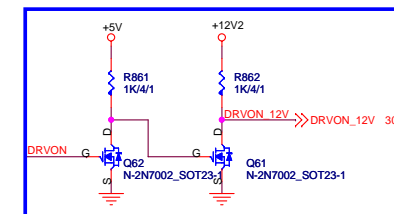
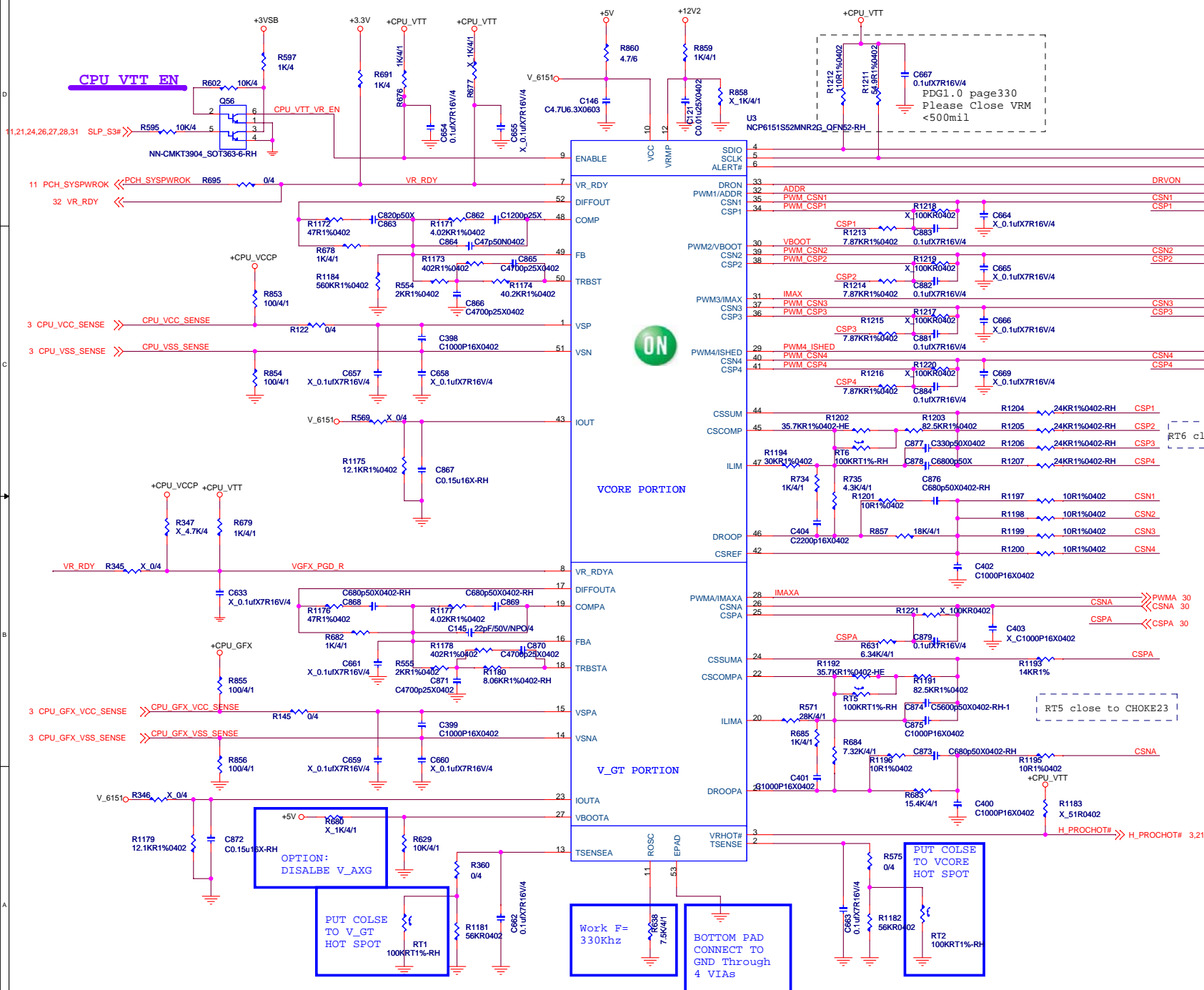
+CPU GFX Output caps

MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

Title: **+1.05V_ME+3.3V_ME+1.05V+1.8V**

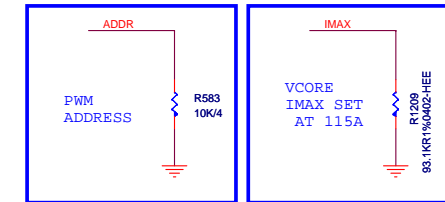
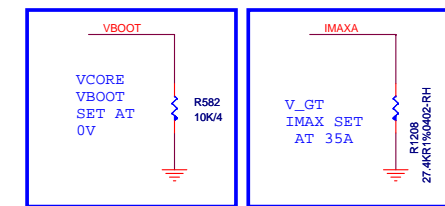
Size: Document Number **MS-7777N1** Rev **10**

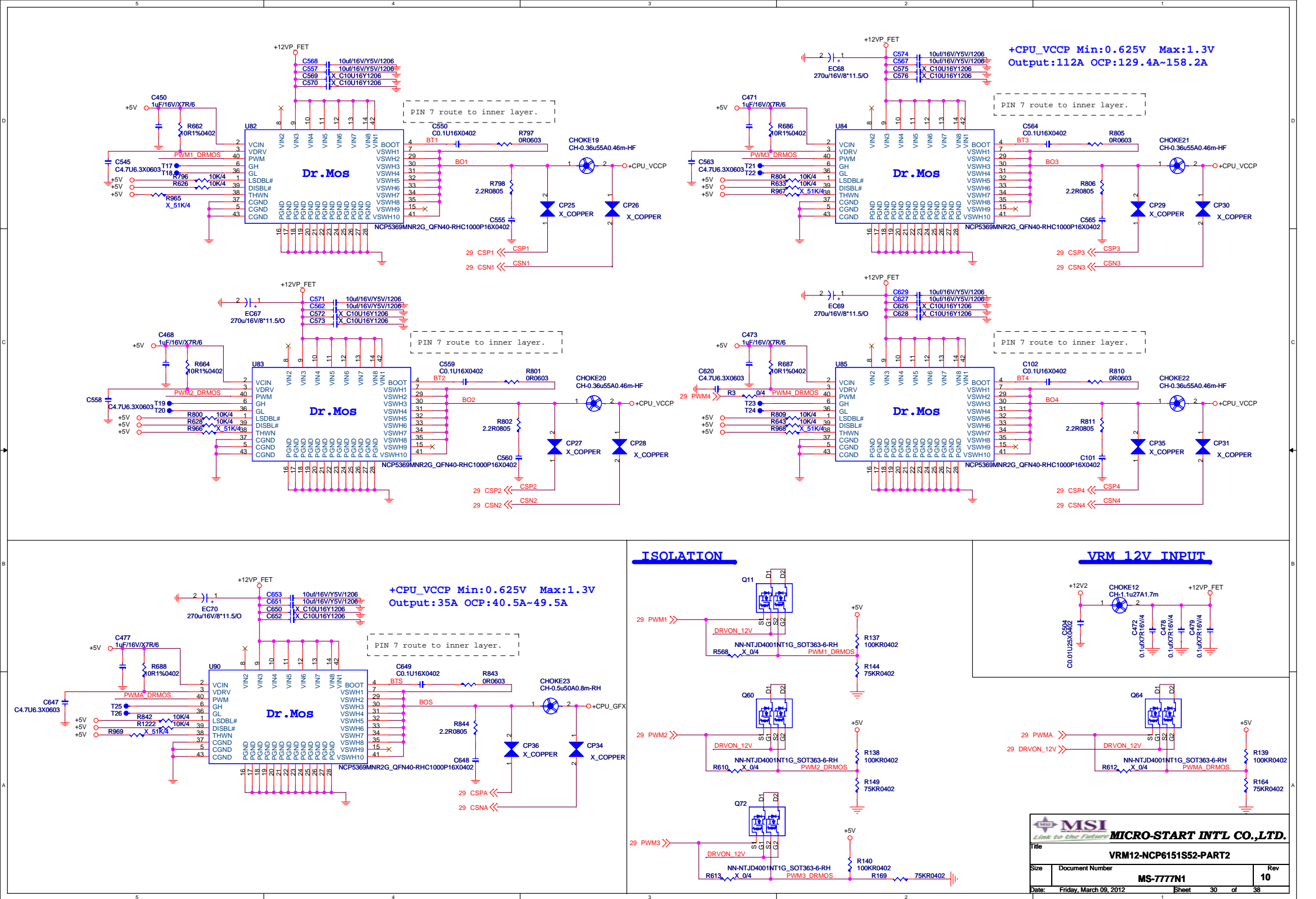
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PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.85V
45K	0.9V
70K	0.95V
95K	1V
125K	1.1V
165K	1.5V





Battery Unit(MS-4295N1)/MB Power Connector

21 PS_ON#_SIO >> PS_ON#_SIO
10,25 ATX_PWROK >> ATX_PWROK

+5VSB_ATX +5V

R848 X.22KR0402
X.10KR0402 R817

C551 X.1u6/3V4
C554 C0.1u16V0402

PWRCONN1

1 12V2
2
3 12V2
4 12V2
5 12V2
6 12V1
7 12V1
8 12V1
9 12V1
10 5VSB
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20

C635 C0.1u16V0402 +12V2
C634 C0.1u16V0402 +12V2
C636 C0.1u16V0402 +12V2
C639 C0.1u16V0402 +12V2
C546 C0.1u16V0402 +12V1
C625 C0.1u16V0402 +12V1
C630 C0.1u16V0402 +12V1
C631 C0.1u16V0402 +12V1
C632 C0.1u16V0402 +12V1
C624 C0.1u16V0402 +5VSB_ATX

PWRCONN20_P_WHITE-1

By-pass caps

+12V2 +12V1 +12V2

C551 10u/16V/75V/1206
C552 10u/16V/75V/1206
C553 10u/16V/75V/1206
C554 10u/16V/75V/1206

Second OVP protection circuit

+5VSB +5VSB +5VSB +5VSB

R245 2KR1%0402 OVP_VCCP
R243 1KR1%0402
R340 2KR1%0402 OVP_GFX
R246 1KR1%0402
R242 2KR1%0402 OVP_VTT
R357 1KR1%0402
R241 1.65KR1%0402 OVP_DDR3
R338 1KR1%0402

C397 C0.1u16V0402
+CPU_VCCP OVP_VCCP
+CPU_GFX OVP_GFX
+CPU_VTT OVP_VTT
+1.5V_DDR3 OVP_DDR3

U17 LM339D_SOIC14

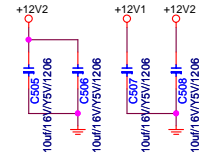
1 VCC
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FOR APS TOOL and Battery Unit(MS-4295N1)

+3VSB_ATX R187 0/4
+3VSB R200 X 0/4

U104

1 10E
2 1A1
3 1A2
4 1A3
5 1A4
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[illegible]

FOR APS TOOL and Battery Unit(MS-4295N1)

The diagram shows the connection between the LV244APWR_TSSOP20-RH and the EC1 connector. The LV244APWR_TSSOP20-RH has pins 1-14 (VCC), 15-18 (GND), 19-22 (VCC), 23-26 (GND), 27-30 (VCC), and 31-34 (GND). The EC1 connector has pins 1-22. The connections are as follows:

- Power Supply:**
 - +3VSB_ATX to pin 1 (VCC)
 - +3VSB to pin 2 (VCC)
 - +3VSB to pin 3 (VCC)
 - +3VSB to pin 4 (VCC)
 - +3VSB to pin 5 (VCC)
 - +3VSB to pin 6 (VCC)
 - +3VSB to pin 7 (VCC)
 - +3VSB to pin 8 (VCC)
 - +3VSB to pin 9 (VCC)
 - +3VSB to pin 10 (VCC)
 - +3VSB to pin 11 (VCC)
 - +3VSB to pin 12 (VCC)
 - +3VSB to pin 13 (VCC)
 - +3VSB to pin 14 (VCC)
 - +3VSB to pin 15 (GND)
 - +3VSB to pin 16 (GND)
 - +3VSB to pin 17 (GND)
 - +3VSB to pin 18 (GND)
 - +3VSB to pin 19 (VCC)
 - +3VSB to pin 20 (VCC)
 - +3VSB to pin 21 (VCC)
 - +3VSB to pin 22 (VCC)
- Signal Connections:**
 - SLP_S3# to pin 1
 - SLP_S4# to pin 2
 - BCU_EXIST# to pin 3
 - PWRBTN# to pin 4
 - SMI#_EC# to pin 5
 - PLTRST#_EC# to pin 6
 - AC_DET# to pin 7
 - SLP_SUS# to pin 8
 - SLP_LAN# to pin 9
 - SLP_S3#_EC# to pin 10
 - SLP_S4#_EC# to pin 11
 - BCU_EXIST#_EC# to pin 12
 - PWRBTN#_EC# to pin 13
 - SMI#_EC# to pin 14
 - PLTRST#_EC# to pin 15
 - AC_DET#_EC# to pin 16
 - SLP_SUS#_EC# to pin 17
 - AC_DET#_EC# to pin 18
- Ground Connections:**
 - Pin 15 (GND) to pin 19 (VCC)
 - Pin 16 (GND) to pin 20 (VCC)
 - Pin 17 (GND) to pin 21 (VCC)
 - Pin 18 (GND) to pin 22 (VCC)

A dashed box indicates the connection to the APS TOOL. The APS TOOL has pins 1-22. The connections are as follows:

- 10,18,21 SERIRQ to pin 1
- 11,18,21 LPC_FRAME# to pin 2
- 12,18 CLK_PCI_KBC to pin 3
- 11,18,21 LPC_AD0 to pin 4
- 11,18,21 LPC_AD1 to pin 5
- 11,18,21 LPC_AD2 to pin 6
- 11,18,21 LPC_AD3 to pin 7
- 10 SCI# to pin 8
- 11,18,21 LPC_AD0 to pin 9
- 11,18,21 LPC_AD1 to pin 10
- 11,18,21 LPC_AD2 to pin 11
- 11,18,21 LPC_AD3 to pin 12
- 10 SCI# to pin 13
- 11,18,21 LPC_AD0 to pin 14
- 11,18,21 LPC_AD1 to pin 15
- 11,18,21 LPC_AD2 to pin 16
- 11,18,21 LPC_AD3 to pin 17
- 10 SCI# to pin 18
- 11,18,21 LPC_AD0 to pin 19
- 11,18,21 LPC_AD1 to pin 20
- 11,18,21 LPC_AD2 to pin 21
- 11,18,21 LPC_AD3 to pin 22

The APS TOOL is labeled "FOR APS TOOL" and "PWRBTN#_EC#".

+12V Discharge

The schematic diagram illustrates a +12V Discharge circuit. It features a +12V1 input connected to a diode D35 (X_Z-UDZS7.5B_SOD323-RH) and a resistor R592 (X_470KR0402). The diode D35 is connected to a MOSFET Q46 (X_N-SST3904_SOT23). The MOSFET Q46 is connected to a resistor R196 (X_470KR0402) and a MOSFET Q23 (X_N-2N7002P_SOT23-3-HF). The MOSFET Q23 is connected to a resistor R539 (X_4.7KR0402) and a resistor R198 (X_680R1206). The resistor R539 is connected to a ground connection G. The resistor R198 is connected to a resistor R244 (X_680R1206) and a capacitor C480 (X_C100550N0402). The capacitor C480 is connected to a ground connection G. The MOSFET Q23 is also connected to a ground connection G. The circuit is labeled '+12V Discharge'.

For EMI reserve

The schematic diagram illustrates the EMI reserve section, featuring a series of components connected to various power rails. The components are labeled as follows:

- Top Rail (12V1):**
 - C584: X, 0.1uF/6V/XSR/4
 - C583: 0.1uX7R16V/4
 - C585: X, 0.1uF/6V/XSR/4
 - C581: 0.1uX7R16V/4
 - C580: X, 0.1uF/6V/XSR/4
 - C582: 0.1uX7R16V/4
 - C579: X, 0.1uF/6V/XSR/4
 - C578: X, 0.1uF/6V/XSR/4
 - C577: X, 0.1uF/6V/XSR/4
 - C608: X, 0.1uF/6V/XSR/4
 - C610: X, 0.1uF/6V/XSR/4
 - C609: X, 0.1uF/6V/XSR/4
 - C599: 0.1uX7R16V/4
- 3.3V Rail:**
 - C598: X, 0.1uF/6V/XSR/4
 - C597: X, 0.1uF/6V/XSR/4
 - C588: X, 0.1uF/6V/XSR/4
 - C589: X, 0.1uF/6V/XSR/4
 - C596: X, 0.1uF/6V/XSR/4
 - C595: X, 0.1uF/6V/XSR/4
 - C594: X, 0.1uF/6V/XSR/4
 - C593: X, 0.1uF/6V/XSR/4
 - C592: X, 0.1uF/6V/XSR/4
 - C591: X, 0.1uF/6V/XSR/4
 - C590: X, 0.1uF/6V/XSR/4
 - C603: X, 0.1uF/6V/XSR/4
- 12V2 Rail:**
 - C918: X, C10p25NM402-RH-2
 - C917: X, C10p25NM402-RH-2
 - C916: X, C10p25NM402-RH-2
 - C915: X, C10p25NM402-RH-2
 - C919: X, C10p25NM402-RH-2
- 12V1 Rail:**
 - C924: X, C10p25NM402-RH-2
 - C923: X, C10p25NM402-RH-2
 - C922: X, C10p25NM402-RH-2
 - C921: X, C10p25NM402-RH-2
 - C920: X, C10p25NM402-RH-2
 - C925: X, C10p25NM402-RH-2
 - C926: X, C10p25NM402-RH-2
 - C927: X, C10p25NM402-RH-2
 - C928: X, C10p25NM402-RH-2
 - C929: X, C10p25NM402-RH-2
 - C930: X, C10p25NM402-RH-2
 - C931: X, C10p25NM402-RH-2
 - C932: X, C10p25NM402-RH-2
 - C933: X, C10p25NM402-RH-2
 - C934: X, C10p25NM402-RH-2
 - C935: X, C10p25NM402-RH-2
 - C936: 0.1uX7R16V/4
 - C937: X, 0.1uF/6V/XSR/4
 - C938: X, 0.1uF/6V/XSR/4
 - C939: 0.1uX7R16V/4
- 3.3V Rail (Bottom):**
 - C607: X, 0.1uF/6V/XSR/4
 - C604: X, 0.1uF/6V/XSR/4
 - C606: X, 0.1uF/6V/XSR/4
 - C605: X, 0.1uF/6V/XSR/4
 - C600: 0.1uX7R16V/4
 - C602: X, 0.1uF/6V/XSR/4
 - C601: X, 0.1uF/6V/XSR/4

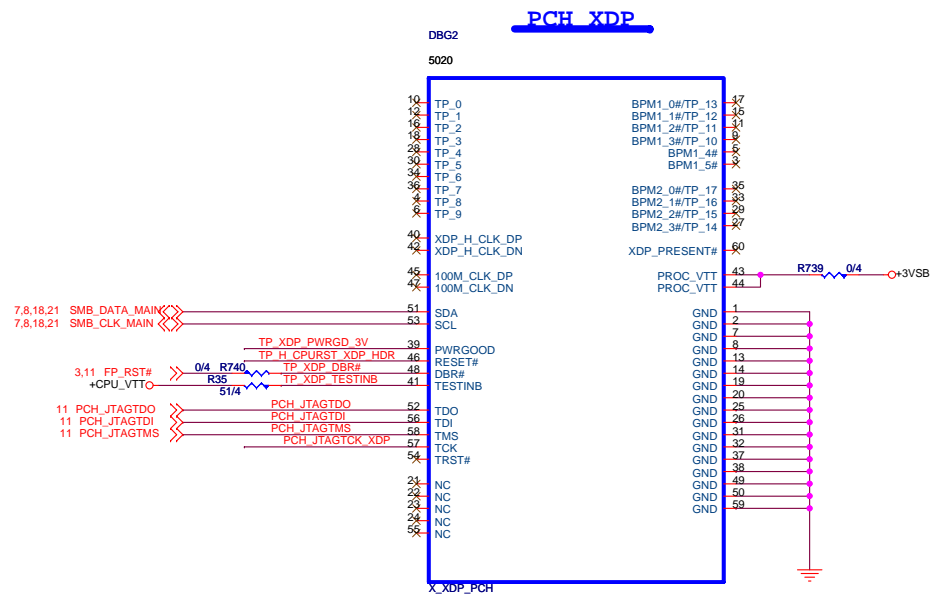
```
RP1-->Between U84 and U85 within 8mm
RP5-->Between U83 and U82 within 8mm
RP3-->Q148within 8mm
RP4-->close U90 within 8mm
RP2-->Q133 within 8mm
RP6-->Q145 within 8mm
RP7-->Q146 within 8mm
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When temperature over 145 degree C,
the value of posistor will be multication.

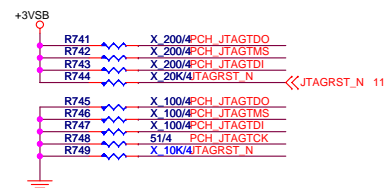


ATX CONNECTOR/OVP/Thermal sense

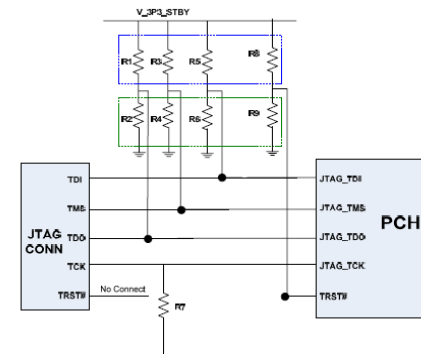
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JTAG PULL HIGH/DOWN



09MOW11



PCH Pin	RefDes	Pre-Production Systems		Production Systems
		ES1	ES2	
TDO	R1	No Stff	200 Ohms	No Stuff
	R2	No Stff	100 Ohms	No Stuff
TDS	R3	200 Ohms	200 Ohms	No Stuff
	R4	100 Ohms	100 Ohms	No Stuff
TMI	R5	200 Ohms	200 Ohms	No Stuff
	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	61 Ohms	61 Ohms	51 Ohms
	R8	20K Ohms	Not Applicable ¹	Not Applicable ¹
TRST#	R9	10K Ohms	Not Applicable ¹	Not Applicable ¹
	R0	Ohms	Not Applicable ¹	Not Applicable ¹

Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes.

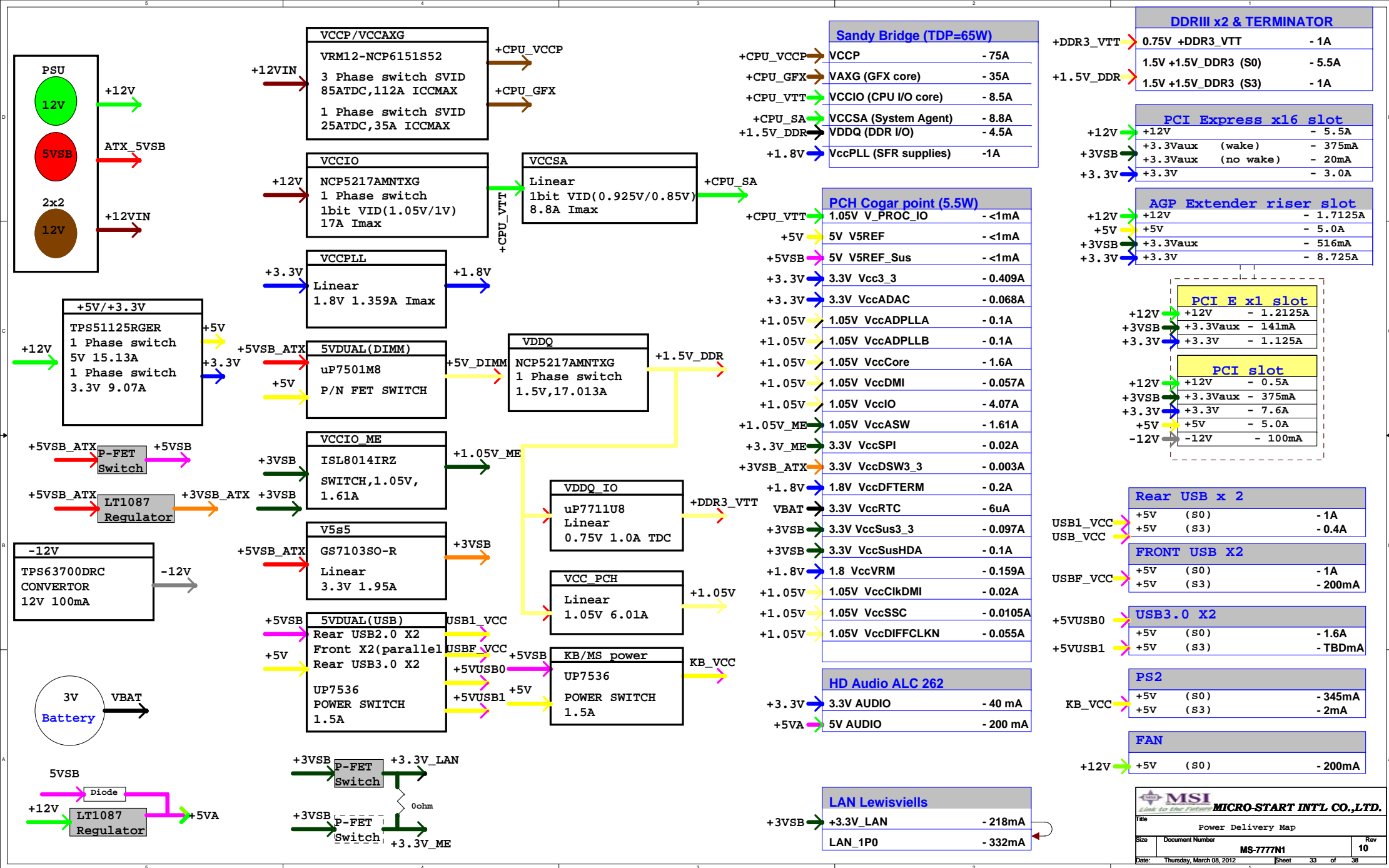


MICRO-START INT'L CO.,LTD.

Title	CPU XDP /PCH XPD
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Size	Document Number	Rev
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PP PCH

GPIO Pin	Type	Default	FUNC/ TYPE	Usage	Extrenal/Internal Pull Up/Down	Power	MUXED/ UNMUXED
GPIO 0	I/O	GPI	I	PCH_GPIO0	EU-10K	+3.3V	
GPIO 1	I/O	GPI	I	SMI# for EC reserve	EU-10K	+3.3V	
GPIO 2	I/O	GPI	I/OD	PCI_IRQ#E	EU-8.2K	+3.3V	
GPIO 3	I/O	GPI	I/OD	PCI_IRQ#F	EU-8.2K	+3.3V	
GPIO 4	I/O	GPI	I/OD	PCI_IRQ#G_ODD	EU-8.2K	+3.3V	
GPIO 5	I/O	GPI	I/OD	PCI_IRQ#H	EU-8.2K	+3.3V	
GPIO 6	I/O	GPI	I	IO_SMI#	EU-10K	+3.3V	
GPIO 7	I/O	GPI	I	SCI# for EC reserve	ED-47K	+3.3V	
GPIO 8	I/O	GPO		FCIM_EN#(No use)	IU-20K	3VSB	UNMUXED
GPIO 9	I/O	Native		USB_OC#_5(No use)	EU-8.2K	3VSB	
GPIO 10	I/O	Native		USB_OC#_6(No use)	EU-8.2K	3VSB	
GPIO 11	I/O	Native	I	PCH_SMBALERT#(No use)	EU-10K	3VSB	
GPIO 12	I/O	Native	O	LAN_DISABLE#	EU-10K	3VSB	
GPIO 13	I/O	GPI	I	SIO_PME#	EU-10K	3VSB	
GPIO 14	I/O	Native		USB_OC#_7(No use)	EU-8.2K	3VSB	
GPIO 15	I/O	GPO		PCH_GPIO15(No use)	EU-10K ID-20K	3VSB	UNMUXED
GPIO 16	I/O	GPI	I	SATA4GP_ODD#	EU-10K	+3.3V	
GPIO 17	I/O	GPI	I	PCH_GPIO17(No use)	EU-10K	+3.3V	
GPIO 19	I/O	GPI	I	SATA1GP(No use)	EU-10K IU-20K	+3.3V	
GPIO 20	I/O	Native	I	PCH_GPIO20(No use)	EU-10K	+3.3V	
GPIO 21	I/O	GPI	I	SATA0GP(No use)	EU-10K	+3.3V	
GPIO 22	I/O	GPI	ODO	PCH_GPIO22(No use)	EU-10K	+3.3V	
GPIO 23	I/O	Native	I	LDRQ1#(No use)	IU-20K	+3.3V	
GPIO 24	I/O	GPO		AMT_LED Debug		3VSB	UNMUXED
GPIO 27	I/O	GPI		PCH_GPIO27(No use)	EU-10K IU-20K	DSW	UNMUXED
GPIO 28	I/O	GPO		OD_PLL_VR_EN(No use)	IU-20K	3VSB	UNMUXED
GPIO 29	I/O	GPI	O	SLP_LAN#		3VSB	
GPIO 30	I/O	Native	I/O	SUSWARN#	EU-10K	DSW	
GPIO 31	I/O	GPI	I/O	PCH_GPIO31(No use)		DSW	
GPIO 32	I/O	GPO	I/O	ECO#		+3.3V	UNMUXED
GPIO 33	I/O	GPO	I	SPI_HOLD#(No use)		+3.3V	
GPIO 34	I/O	GPI	O	PCH_GPIO34(No use)	EU-10K	+3.3V	
GPIO 35	I/O	GPO	ODO	CLR(GPI)	EU-10K	+3.3V	UNMUXED
GPIO 36	I/O	GPI	I	PCH_GPIO36(No use)	ID-20K	+3.3V	
GPIO 37	I/O	GPI	I	PCH_GPIO37(No use)	ID-20K	+3.3V	
GPIO 38	I/O	GPI	ODO	PCH_GPIO38(No use)	EU-10K	+3.3V	
GPIO 39	I/O	GPI	ODO	PCH_GPIO39(No use)	EU-10K	+3.3V	
GPIO 40	I/O	Native		USB_OC#_1[2.0 UP(1)]& 3.0 UP(2)]	EU-8.2K	3VSB	
GPIO 41	I/O	Native		USB_OC#_2[2.0 F_UP(4)]	EU-8.2K	3VSB	
GPIO 42	I/O	Native		USB_OC#_3[2.0 F_UP(5)]	EU-8.2K	3VSB	
GPIO 43	I/O	Native		USB_OC#_4[2.0 R_(8,9)]	EU-8.2K	3VSB	
GPIO 44	I/O	Native	I	PCIECLKRQ5#(No use)	EU-10K	3VSB	
GPIO 45	I/O	Native	I	PCIECLKRQ6#(No use)	EU-10K	3VSB	
GPIO 46	I/O	Native	I	PCIECLKRQ7#(No use)	EU-10K IU-20K	3VSB	
GPIO 48	I/O	GPI	ODO	PCH_GPIO48(No use)	EU-10K	+3.3V	
GPIO 49	I/O	GPI	I	PCH_GPIO49(No use)	EU-10K	+3.3V	
GPIO 50	I/O	Native	I	PCI_REQ#1	EU-8.2K	+3.3V	
GPIO 51	I/O	Native	O	PCI_GNT#1	IU-20K	+3.3V	
GPIO 52	I/O	Native	I	PCI_REQ#2(No use)	EU-8.2K	+3.3V	
GPIO 53	I/O	Native	O	PCI_GNT#2(No use)	IU-20K	+3.3V	
GPIO 54	I/O	Native	I	PCI_REQ#3(No use)	EU-8.2K	+3.3V	
GPIO 55	I/O	Native	O	PCI_GNT#3(No use)	IU-20K	+3.3V	
GPIO 57	I/O	GPI		PCH_GPI57(No use)	ED-47K	3VSB	
GPIO 58	I/O	Native	I/OD	PCH_SML1CLK	EU-2.2K	3VSB	UNMUXED
GPIO 59	I/O	Native		USB_OC#_0[2.0 DOWN(0)&3.0 DOWN(1)]	EU-8.2K	3VSB	
GPIO 60	I/O	Native	ODO	PCH_SML0ALERT#(No use)	EU-2.2K	3VSB	
GPIO 61	I/O	Native	O	LPCPD#(No use)	IU-20K	3VSB	
GPIO 62	I/O	Native	O	SUSCLK for SIO		3VSB	

GPIO Pin	Type	Default	FUNC/ TYPE	Usage	Extenal/Internal Pull Up/Down	Power	MUXED/ UNMUXED
GPIO 63	I/O	Native	O	SLP_S5#		+3.3V	
GPIO 64	I/O	Native	I/O	NC	ID-20K	+3.3V	
GPIO 65	I/O	Native		NC	ID-20K	+3.3V	
GPIO 66	I/O	Native	O	NC	ID-20K	+3.3V	
GPIO 67	I/O	Native		CLK14M_SIO for SIO CLK	ID-20K	3VSB	
GPIO 68	I/O	Native		SATA_ODD_PWRCTL	EU-10K	+3.3V	
GPIO 69	I/O	Native		NC		+3.3V	
GPIO 70	I/O	Native		PCH_GPIO70(No use)	EU-10K	+3.3V	
GPIO 71	I/O	Native		PCH_GPIO71(No use)	EU-10K	+3.3V	
GPIO 72	I/O	Native	I	PCH_GPIO72(No use)	EU-10K IU-20K	3VSB	UNMUXED
GPIO 74	I/O	Native	ODO	PCH_SML1ALERT#(No use)	EU-10K	3VSB	
GPIO 75	I/O	Native	I/OD	PCH_SML1DATA	EU-2.2K	3VSB	

(M)=Mobile combine

DSW=Deep Sleep Well (+3VSB_ATX)

(5)=Internal pull up/down 20K,disable after RSMRST# deassert.

(4)=Internal pull up/down 20K,disable after PLTRST# deassert.

(3)=Pull up/down enable only in DS4/DS5.

(2)=Pull down enable when pwrok is low.

(1)=Pull down is not enable when pwrok is low.

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
Riser slot (PCI1)	PIRQ#F(INTA#) PIRQ#C(INTB#) PIRQ#H(INTC#) PIRQ#E(INTD#)	PREQ#1 PGNT#1	AD17	CLK33M_PCI_SLOT

DDR3 DIMM Configuration

DEVICE	ADDRESS	CLOCK
DIMM 1	0A2H	MEM_MA_CLK_H1/MEM_MA_CLK_L1 MEM_MA_CLK_H0/MEM_MA_CLK_L0
DIMM 2	0A4H	MEM_MB_CLK_H1/MEM_MB_CLK_L1 MEM_MB_CLK_H0/MEM_MB_CLK_L0

SMBus Distribution

SMBus	Power	Load
SMBCLK	VCC3_SB	MEM_VREFDQ,PCH,PCIEX16,PCIEX1,PCI,OW
SMBCLK_ISO	VCC3	DIMM, CLK GEN, XDP,PSU

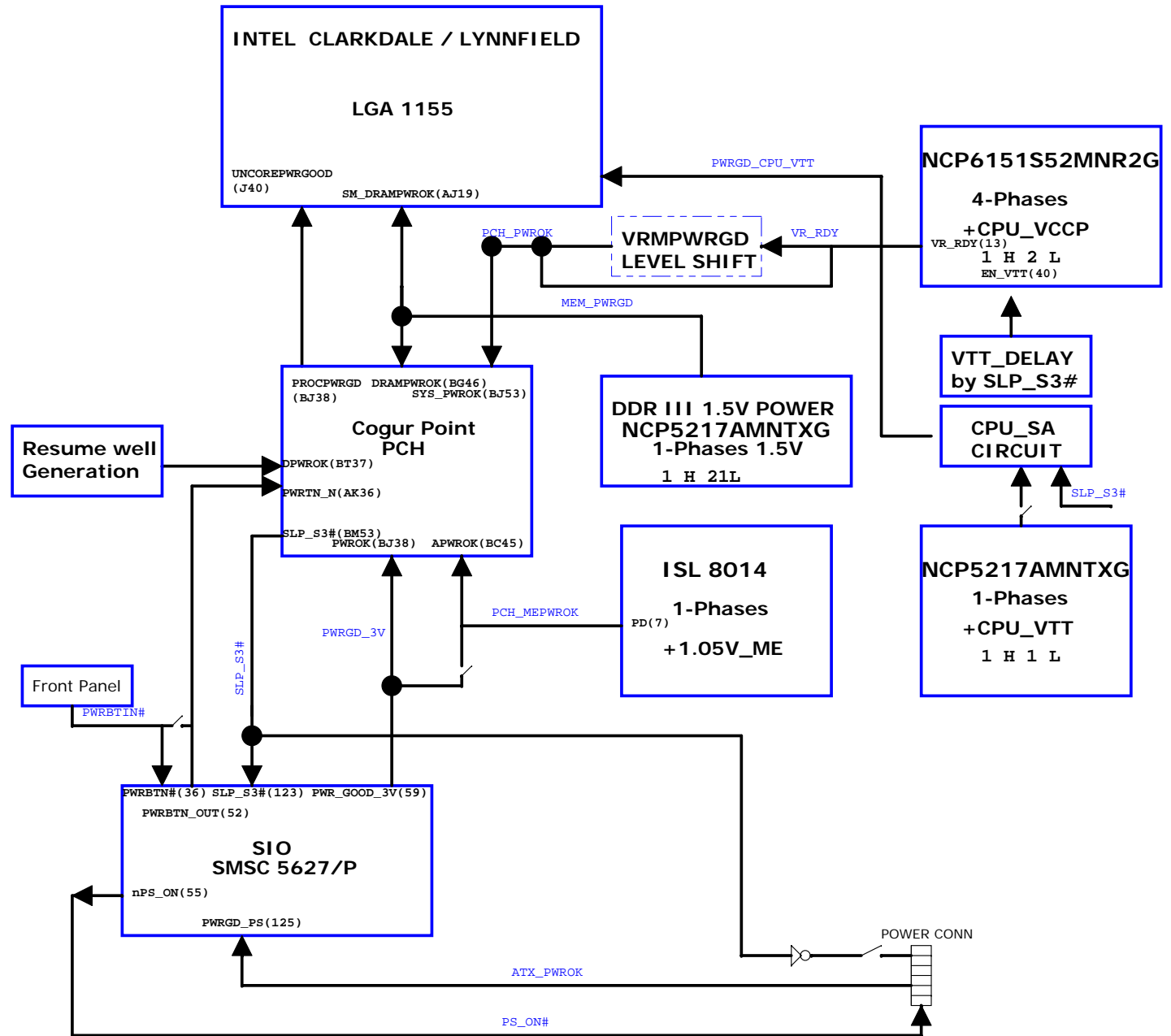
Jumper Setting

JBAT1	(1-2)Normal	(2-3)Clear CMOS	
MEDEBUG1	(1-2)short: Normal	(2-3)short:ME Disable for FPROG	
J3	(1-2)short: Normal	(1-2)Open: Clear PW	
JME1	(1-2)Normal	(2-3)Clear ME RTC	(un-mount)

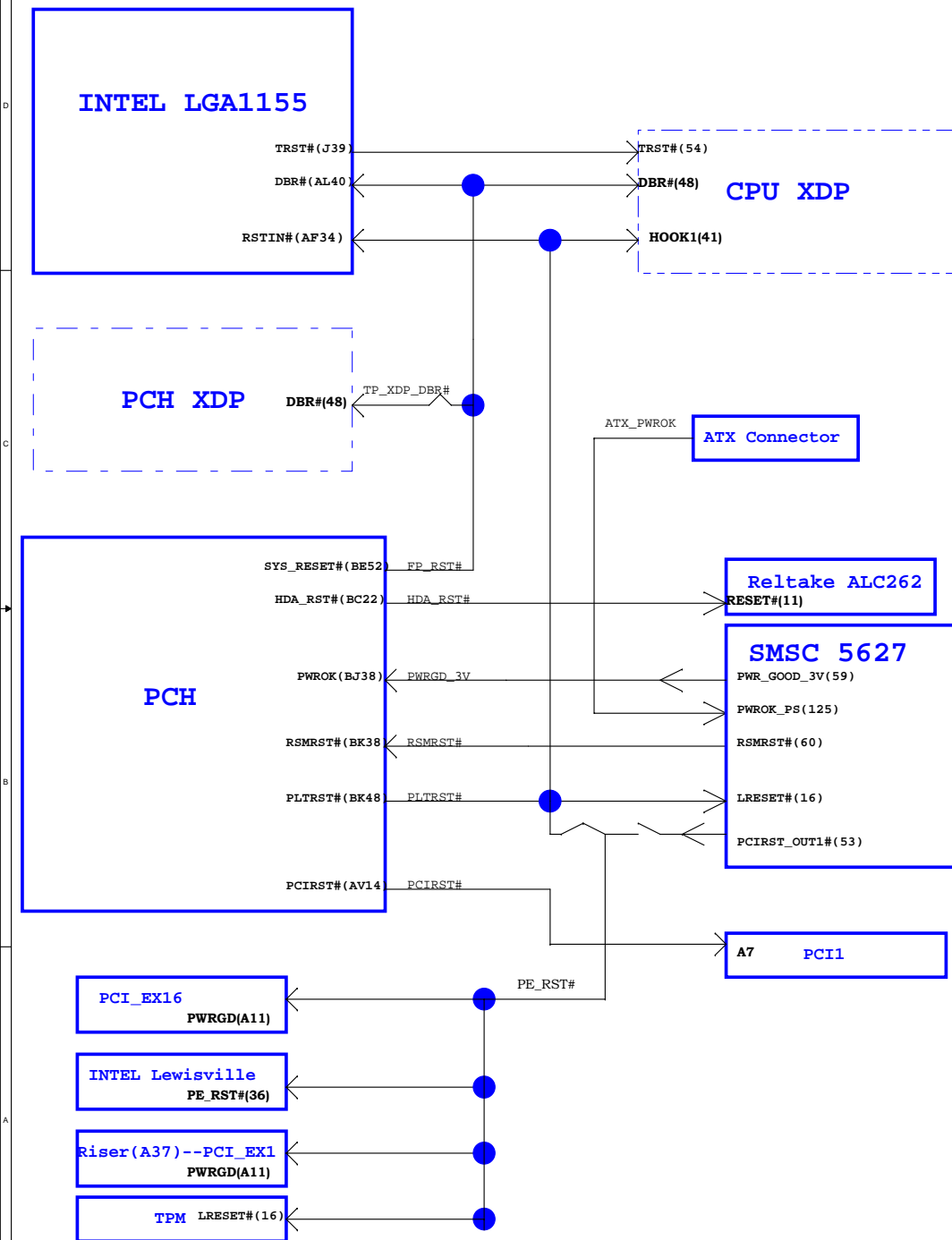
SIO - SMSC-5627P Configuration

PIN NAME	PIN#	USAGE	Input/Output
GP036/SMB_CLK1	72	SMB_CLK1	INPUT
GP040/SMB_DATA1	74	SMB_DATA1	INPUT
nLED1/GP006	25	POWER LED	OUTPUT
nLED2/GP007	26	SUSPEND LED	OUTPUT
GP071/nIO_SMI	128	IO_SMI#	OUTPUT
PECI/LVSMBC/GP072	32	PECI	INPUT
TACH1/GP017	39	TACH1	INPUT
TACH2/GP020	40	TACH2	INPUT
TACH3/GP021	41	TACH3	INPUT
GP022/PWM1	49	PWM1	OUTPUT
GP023/PWM2	50	PWM2	OUTPUT
GP024/PWM3	51	PWM3	OUTPUT
PROCHOTIN/OUT/GP16	38	PROCHOTIN	INPUT
GP042 / DRVDE0	78	DRVDE0	OUTPUT
GP041 / IO_PME#	77	IO_PME#	OUTPUT
GP047 / TXD1	102	TXD1	OUTPUT
GP063 / KBDRST#	120	KBDRST#	OUTPUT
GP064 / A20M	121	A20M	OUTPUT
PWRBTN# /GP15	36	PWRBTN#	INPUT
GP25/PWRBTN_OUT#	52	PWRBTN_OUT#	OUTPUT
GP05/PECI_REQUEST#	22	PECI_REQUEST#	OUTPUT
GP012/LAN_WAKE#	29	LAN_WAKE#	OUTPUT
GP013/VSB_CTRL	30	VSB_CTRL	OUTPUT

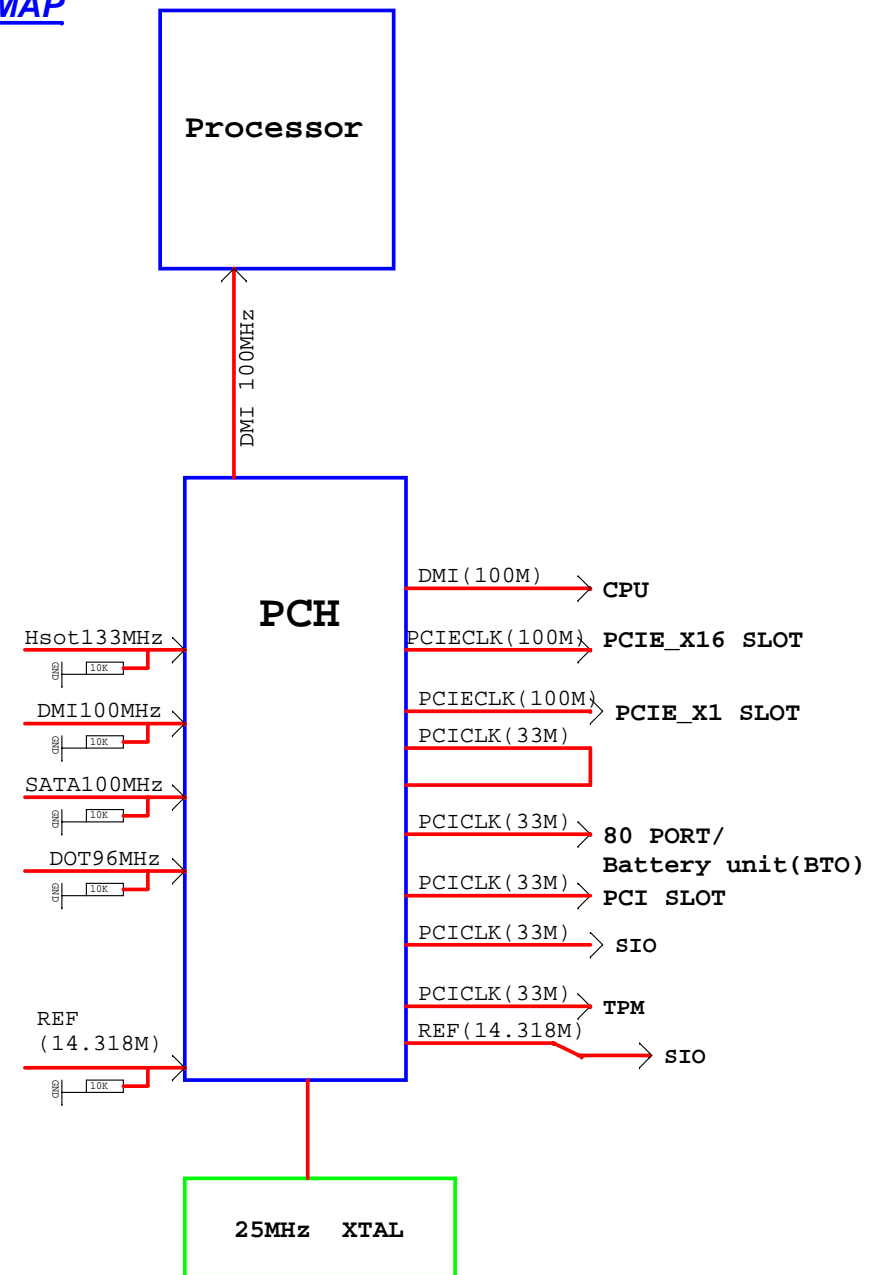
PWROK MAP



RESET MAP



CLOCK MAP



Board Stack-up (6 layers)

(1080 Prepreg Considerations)

Palomar stackup requirem ents	Plane Description	Thickness (mils)	min	max
	solder mask	0.05	0.1	1.2
Signal 1	SIGNAL	1.9	1.1	2.75
	prepreg	2.7	2	3.5
Plane 2	POWER	1.2	1	1.4
	core	4.0	3.25	4.75
Signal 3	SIGNAL	1.2	1	1.4
	core	3.9	1	1.4
Signal 4	SIGNAL	1.2	1	1.4
	core	4.0	3.25	4.75
Plane 5	GND	1.2	1	1.4
	prepreg	2.7	2	3.5
Signal 6	SIGNAL	1.9	1.1	2.75
	solder mask	0.05	0.1	1.2

Intel spec:	min	62.3	max
Total thickness (mils):	57	62	70

Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 90ohm : 15/4.5/7.5/4.5/15
PCIe - 80ohm : 16/5/5/16
SATA(stripline) - 90ohm : 15/4.5/6.5/4.5/15
DVI : 20/4/6/4/20
USB3.0: 16/5/5/16
FDI : 16/5/5/16
DMI: 16/5/5/16

Example Fab Drawing Note (1080 Prepreg PCB)

Trace Width (mils)	Differential Spacing (mils)	Target Impedance	Tolerance
4.0	NA	50-ohm,single-ended	15%
6.5	NA	40-ohm,single-ended	15%
7.5	NA	37-ohm,single-ended	15%
9.5	NA	32-ohm,single-ended	15%
3.9	8.1	95-ohm,differential	20%,reference only
4.5	7.5	90-ohm,differential	20%,reference only

Processor Impedance Requirements by Interface

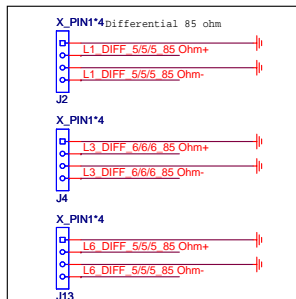
Interface	Impedance Required
DDR3 (CLK,CLK#)	36 Ω single-ended
DDR3 (DQ,DQS,ECC)	40 Ω single-ended
DDR3 (Control)	36 Ω single-ended
DDR3 (Command)	32 Ω single-ended
PCI Express* 2.0	80 Ω differential
DMI	85 Ω differential
FDI	85 Ω differential
VGA	37 Ω single-ended at PCH breakout, then 50 Ω single-ended to VGA connector

PCH Impedance Requirements by Interface

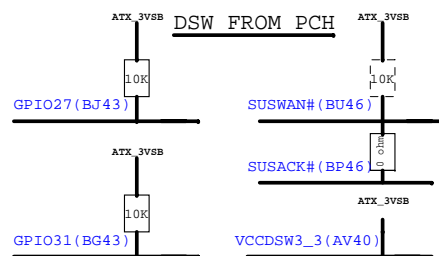
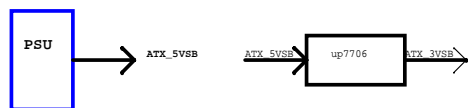
Interface	Impedance Required
PCI	50 Ω single-ended
Miscellaneous	50 Ω single-ended
PCI Express* 2.0	80 Ω differential
SATA	90 Ω differential
USB	90 Ω differential

USB3.0 85 ohm differential

IMPEDANCE MEASUREMENT

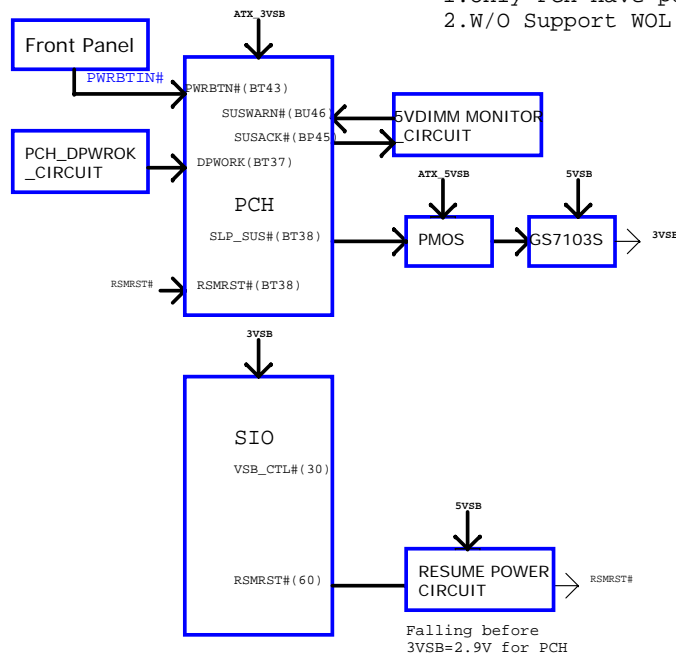


DSW POWER DELIVERY CONCEPT

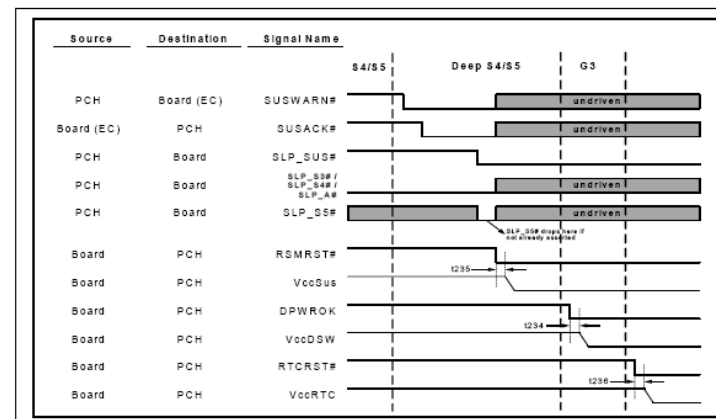


DSW FROM PCH

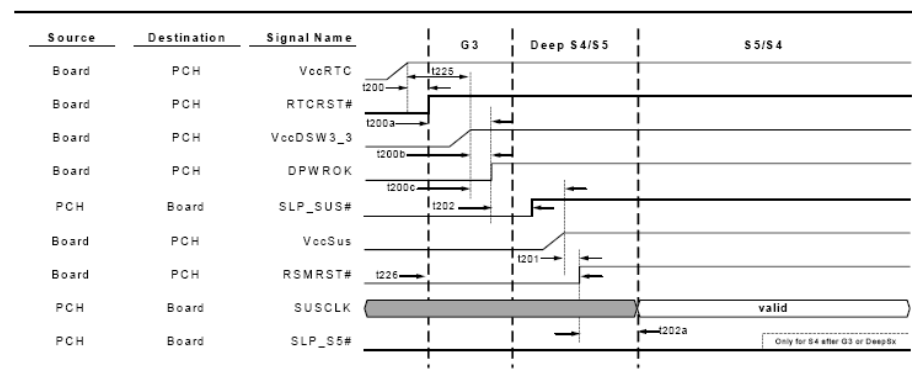
ME102 presentation
1. Only PCH have power consumption (5~10mA).
2. W/O Support WOL (INTEL PHY).



S4/S5 to Deep S4/S5 to G3 w/ RTC Loss Timing Diagram



G3 w/RTC Loss to S4/S5 (With Deep S4/S5 Support) Timing Diagram



MS-6XXXN1	ERP Number	Function
MS-7777-0C	601-7777-C10	Mainboard
MS-4046-2A	604-4046-020	Power Button/LED board
MS-4213-10	604-4213-020	Front Audio Board
MS-4048-50	604-4048-060	Front USB Board
MS-4266-10	604-4266-010	Riser Card
MS-4220-10	604-4220-010	Print Port Riser Board
MS-4295-0C	604-4220-C10	Battery Unit (BTO)